Wild River Technology Signal Integrity Training

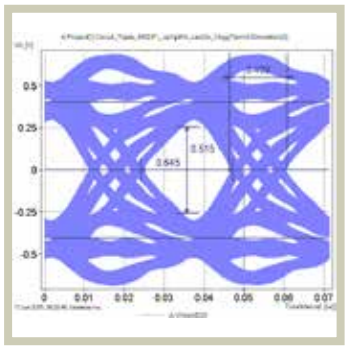
wild river technology

Reduce Risk – Design with Greater Confidence – Develop Better Design Methodologies – Reduce Fab Spins

Wild River Technology (WRT) training classes are offered either on site or web based, and are available at select locations on the West Coast, including Portland, Oregon and the Bay Area of California. Contact WRT for information regarding the class or check our website for upcoming dates. We offer in-house classes per customer requirements. Contact

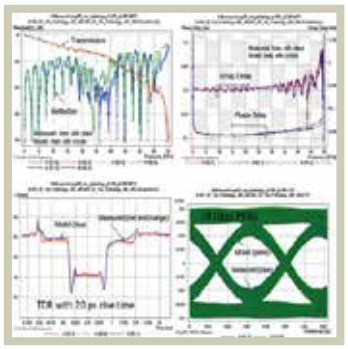
www.wildrivertech.com

Pursuing the Art of Signal Integrity



- De-embedding
- Channel Modeling Concepts
- Improve Design Confidence

- Simulation to Measurement
- EDA Jitter Analysis
- Material Identification



- Advanced Jitter
- Compliance
- Stochastic Analysis – Jitter Math

The WRT training process:

1. Check with WRT Sales or our web site for upcoming public classes or schedule private training for your company. Also, if you register on our web site you will receive the WRT newsletter which will keep you up to date on upcoming public classes.

2. Contact WRT Sales for additional information and/or to book training. For public classes you can also go directly to the WRT website, click on the Events section, and sign up.

3. Once you are enrolled an extensive bibliography of IEEE, DesignCon, textbooks, and assorted material will be sent to you before the class begins. WRT will suggest reading text chapters and specific papers prior to the class.

4. Attendees should come prepared with questions, including ongoing projects. Check with corporate legal and management prior to asking non-generic detailed questions.

Wild River Technology Signal Integrity Training

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WRT classes provide:

- Theory and foundation material required to grasp fundamental concepts and develop an intuitive understanding.
- Practical knowledge, equipping the S.I. engineer with a clear path and plan of addressing challenging signal integrity problems.

Standard Product Classes Offered

Contact WRT for prices

CLASS NO.	TITLE	PRICE
JITT-01	10G BASE KR	
JITT-02	100G Ethernet Signaling	
JITT-03	Advanced Crosstalk and Peak Distortion Analysis, Conquering Difficult SI	
JITT-04	Get up to Date in High Speed Tech: COM, ICN, eTJ, eBUJ	
JITT-05	Channel Optimization by Combining Modeling and Measurement	
JITT-06	Advancing to the Edge: 56G design, compliance, and debug	
SI-01	Jitter Analysis Essentials for Signal Integrity Engineers	
SI-02	Mastering High Speed I/O: compliance, diagnostics, and simulation	
SI-03	Understanding, Debugging, and Testing High Speed I/O	
SI-04	Advanced TDR and VNA Measurement Methodology	
SI-05	WRT Channel Modeling for advanced EDA to Measurement Correspondence	
SI-06	Introduction into computational electromagnetics for interconnect analysis	
SI-07	Multiport theory for interconnect analysis	
SI-08	Analysis of signal propagation in interconnects	
SI-09	Simbeor EDA Training	
ADS-01	Advanced Time-domain analysis (TDR/TDT) Using Keysight ADS	
ADS-02	Advanced ADS for Signal Integrity Engineers	
TDR-01	TDR Basics	
TDR-02	TDR Based Modeling Using Tektronix' IConnect	

SI-01: Jitter Analysis Essentials for Signal Integrity Engineers – 1 day

Instructor – Ransom Stephens, Ph.D

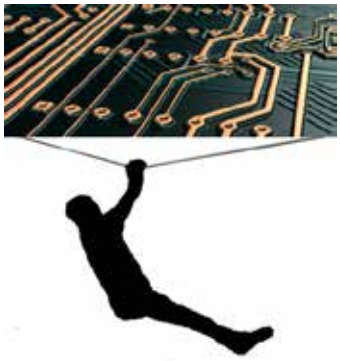
- Fundamentals of eye diagram, jitter, noise, and BER analysis on multi-gigabit signals
- Understanding random & deterministic and correlated & uncorrelated jitter and noise
- Recognize the causes and signs of jitter and noise in eye diagrams and on waveforms
- Introduction to differential signaling, clock recovery, NRZ, and PAM4
- Simplifying differential S-parameter analysis for common backplane channels
- Introduction to skin effect, dispersion, and channel response
- Channel Characterization Primer: Oscilloscope and BERT techniques
- 45 minute open discussion scheduled at end of day

SI-02: Mastering High Speed I/O: compliance, diagnostics, and simulation—1 day

Instructor – Ransom Stephens, Ph.D

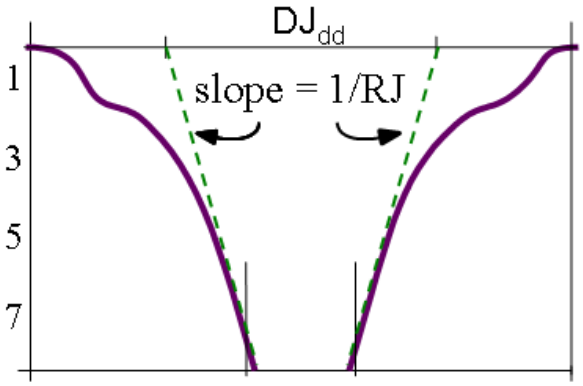
Prerequisite: Signal Integrity Essentials

- Expert jitter and noise analysis—RJ, DJ, DDJ, ISI, SJ, PJ, HPBJ, DCD, BUJ, E/OJ—including the dual-Dirac model, Q-scale, bathtub plots, and TJ, Eye Height/Width
- Forward clocking and clock recovery
- Patterns CJPAT, clock-like, …
- Exploration of channel pathological space (loss, resonance, mode issues, crosstalk)
- The pros and cons of PAM4, ENRZ, and when to switch from NRZ
- Introduction to simulation methods, IBIS-AMI, ADS techniques
- High speed serial technology overview: OIF-CEI 3.1, 100/400 GbE, PCIe 2-4, USB3.1, 32GFC, etc.
- Selection of Capital equipment, trade-offs, tips, and methodology
- Oscilloscope, BERT, Phase noise analyzer methods of jitter analysis



SI-03: Understanding, Debugging, and Testing High Speed I/O—2 days

Instructor – Ransom Stephens, Ph.D

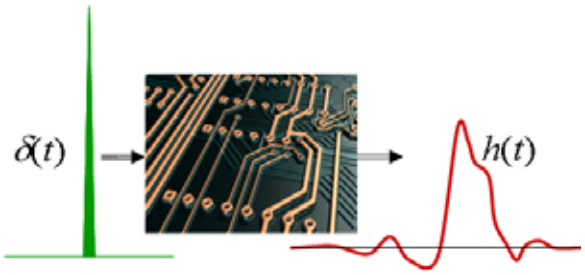


Prerequisite: Signal Integrity Essentials

- Jitter, noise, crosstalk, serdes and interconnect test techniques
- Understand the dual Dirac Model, Total Jitter, Eye Width/Height, BER contour
- Dispersion, skin effect and inter-symbol interference
- Thinking in S-parameters: differential/common modes, ISI, crosstalk
- Equalization techniques at the transmitter and receiver: pre/de-emphasis, CTLE, FFE, DFE
- PAM4 signaling and diagnostic differences with NRZ/PAM2
- High speed metrology, embedding/de-embedding
- Developing a hardware debug strategy (aka, Jitter, Noise, and Error Analysis)

JITT-01: 10G BASE KR—1 day

Instructor – Ransom Stephens, Ph.D

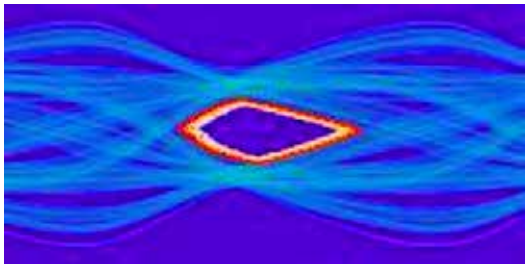


Prerequisite: Signal Integrity Essentials

- Review jitter concepts….
- Technical overview of 802.3bj specification
  - Loss, Insertion Loss and Insertion Loss deviation
  - Crosstalk, MDNEXT, MDFEXT, FEXT, NEXT
  - Integrated crosstalk ratio (ICR)
- Serial Link analysis approach

JITT-02: 100G Ethernet Signaling—1 day

Instructor – Ransom Stephens, Ph.D



Prerequisite: Signal Integrity Essentials

- All the details of 802.3bj, OIF-CEI 3.1
- Techniques for diagnostic and compliance measurements of serdes and interconnects
- S-parameters, pulse modeling, and masks
- Receiver tolerance testing
- FEC, its limitations, the PCS gearbox, multi-signal clocking, and interplay with DFE
- Oscilloscope, TDR, VNA, BERT
- Advanced preview of 56G

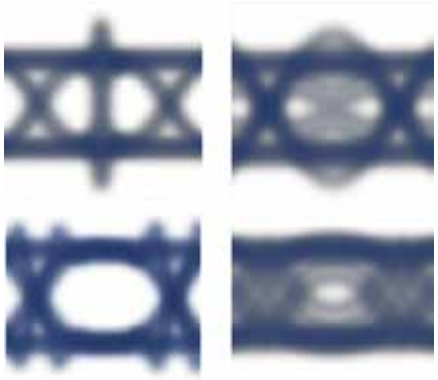
JITT-03: Advanced Crosstalk and Peak Distortion Analysis, Conquering Difficult SI – 1 day

Instructor – Ransom Stephens, Ph.D

Prerequisite: pre-req: Mastering High Speed I/O

- Peak distortion analysis—pulse response, transfer functions, BER contours and bathtub plots
- EMI and electrodynamics of crosstalk: synchronous/ asynchronous, spectra, pulse-response
- Crosstalk from the S-parameter and TDR perspectives
- Diagnosing crosstalk problems with waveforms and eye diagrams
- FEXT, NEXT, MDFEXT, MFNEXT, ICN, and interference tolerance testing
- Equalization in the presence of crosstalk—optimizing CTLE, FFE, DFE and clock recovery

(aka Advanced crosstalk and PDA)



JITT-04: Get up to Date in High Speed Tech: COM, ICN, eTJ, eBUJ—1 day

Instructor – Ransom Stephens, Ph.D

Prerequisite: Mastering High Speed I/O or Understanding, Debugging, and Testing High Speed I/O

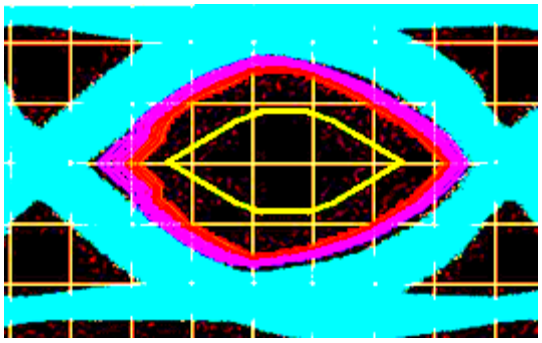
- Closed eye analysis: effective jitter and noise independent of channel response
- Jitter and noise analysis techniques: tail-fitting, spectral fitting, aperiodic BUJ
- Embedding and de-embedding channels, noise sources, equalization, clock recovery, etc.
- How to calculate, measure, and simulate COM
- Understanding ICN measurements and options

(aka, COM)

JITT-05: Channel Optimization by Combining Modeling and Measurement – 1 day

Instructor – Ransom Stephens, Ph.D

- Designing good signal integrity into your test fixtures
- Primer on Launch design
- De-embedding approach overview, compromises
- S-parameter, making good measurements to 50GHz
- S-parameter quality work flow
- Qualitative and quantitative techniques for comparing simulations and measurements
- Understanding statistical and systematic uncertainties and model-dependent biases



(aka, Primer on Channel Optimization Strategies – EDA and Measurement Approach)

SI-04: Advanced TDR and VNA Measurement Methodology—1.5 days

Instructor – Alfred P. Neves

Prerequisite: Mastering High Speed I/O

- Fourier analysis and the essential equivalence of the time and frequency domains
- Understand the concept of reference plane versus S-parameter measurement
- Adapters for measurement - cleaning, operation
- Set up calibration based on DUT characteristics - insert-ability, reciprocity, DUT characteristics, etc.
- Examine and review Touchstone format of S-parameter files
- Operation of VNA - averaging, smoothing, sample points, group delay
- VNA set up for 3D EM analysis
- Calibrate VNA for 1, 2 and 4 ports with both Electronic calibration, and manual SOLT kit
- Validate 1, 2, and 4 port calibrations
- Resolve sticky calibration issues... what do I do when I cannot adequately calibrate?
- Create 2 and 4 port S-parameters (Smn, and mixed-mode such as SDD21), interpreting mixed-mode
- Understand key error sources in VNA, and relate them to DUT characteristics
- Make multi-port S-parameters for crosstalk analysis
- Correspond S-parameter measurement to TDR, or time domain methods. Note: This is optional based on customer having Transform Option in VNA, or PLTS, optionally customer can use Matlab RF Toolbox.
- S-parameter work flow for passivity/causality and determine root causes of problems
- Time domain simulation of S-parameters considerations, distortion and tilt in time domain along with getting good D.C. point
- Resampling, Broadband Spice and Rational Compact Modeling of S-parameters

JITT-06: Advancing to the Edge: 56G design, compliance, and debug

1 day presentation, 1 hour open discussion

Instructor – Ransom Stephens, Ph.D

Prerequisite: Mastering High Speed I/O

- Where to find what you need in the specs and how to use and understand it
- Skin effect, dispersion, and PCB nuances at very high data rates
- Advanced equalization methods
- Crosstalk, BER and jitter/noise analysis on PAM4 signals

SI-05: WRT Channel Modeling for advanced EDA to Measurement Correspondence

(aka, 56Gbpsec – architectures, approaches, materials and design) – ¾ day presentation, open discussion and question session included

Instructor – Alfred P. Neves

What the class is about: Achieve stellar EDA simulation to measurement correspondence out to 70GHz! This class combines hands-on training with a brief classroom discussion and is typically tailored to a specific customer need and available test equipment. Since applications of WRT channel modeling products vary greatly, class material is selected in an al-carte fashion. This class is offered for WRT Channel Modeling customers.

Overview of CMP design.

- SE lines
- Diff Structures
- VIA designs
- crosstalk aggressors and mode conversion
- resonators
- graduated coplanar
- stepped impedance
- forward coupler

- Understand the concept of primitive structure in relationship to other test structures, and Channel Modeling hierarchy.
- Reconfigurable backplane concept - integrating structures
- Calibration approaches - Unknown THRU, Automatic Fixture Removal (for customers with PLTS with OPTION -5), TRL/LRM, T-matrix de-embedding
- Set up calibration based on DUT characteristics - insert-ability, reciprocity, DUT characteristics, etc.
- Measure Touchstone format of S-parameters of single-ended and differential structures
- Analyze crosstalk aggression in frequency/time domain, NEXT, FEXT, ICR, possibly measure eye diagram jitter at a specified data rate (requires BERT, and appropriate sampling or real time oscilloscope.
- Concepts of calibration verification using resonant structures - averaging, smoothing, sample points, group delay

- Validate 1, 2, and 4 port calibrations.
- Identification of material properties
- Correspond S-parameter measurement to TDR of . Note: This is optional based on customer having Transform Option in VNA, or PLTS, optionally customer can use Matlab RF Toolbox.

Duration: The class duration is 1 business day, typically starting at 10pm and ending 5pm.

SI-06: Introduction into computational electromagnetics for interconnect analysis
2 hours duration

Instructor – Yuriy Shlepnev, Ph.D

- Introduction into Electromagnetics
- Computational Electromagnetics (CEM)
- Static and Quasi-Static Problems
- Time-Domain Electromagnetics
- Frequency-Domain Electromagnetics
- Partial Differential Equations Based Methods
- Integral Equation Based Methods
- Combined and Hybrid Methods

SI-07: Multiport theory for interconnect analysis - 2 hours duration

Instructor – Yuriy Shlepnev, Ph.D

- Basics of S-parameters
- Frequency-domain analysis with S-parameter models
- Time-domain analysis with S-parameter models
- Quality of S-parameter models

SI-08: Analysis of signal propagation in interconnects - 2 hours duration

Instructor – Yuriy Shlepnev, Ph.D

- Signal degradation factors
- De-compositional electromagnetic analysis
- Modeling transmission lines
- Modeling via-holes and other discontinuities

SI-09: Simbeor EDA Training

1.5hours/week for 12 week duration, classes are recorded for absentees benefit

Instructor – James Bell

This is a series of 1 hour on-line classes developed to bring the student up to full speed on the Simbeor tool. Questions during the class are encouraged, as we will be taking small bytes each session. This class requires several hour/week of commitment to complete working assignments. Wild River Technology Channel Modeling platforms are used as basis of physical layer.

- Session 1: De-compositional analysis and the Electromagnetic Simulation Environment, and Getting around the Simbeor GUI.
- Session 2: Defining Materials and Stack-up
- Session 3: Model creation wizards - Transmission line models, Differential via-hole models creation, and Single via-hole models
- Session 4: Import of Touchstone models, Circuits and Simulations
- Session 5: End-to- end interconnects analysis with linear solver
- Session 6: Outputting model files
- Session 7: Multilayered circuits editing - Geometry creation and editing, Symmetry, and Simulation area and the lattice box
- Session 8: Geometry import and auto-decomposition
- Session 9: Rational compact and SPICE macro-models
- Session 10: Time-domain analysis (TDR/TDT)
- Session 11: Import and simulation of PCB designs
- Session 12: Using the SI Tune tool
- Session 13: Using the Eye Analyzer tool

ADS-01: Advanced Time-domain analysis (TDR/TDT) Using Keysight ADS - 6 hrs

Instructor – Tim Wang Lee

- Ways to produce time domain response in ADS and the caveats
- Creating Measurement-based model with ADS
- Material properties extraction with ADS TDR

ADS-02: Advanced ADS for Signal Integrity Engineers – 2 Days - 2 Days

Instructor – Tim Wang Lee

Review:

- Advanced UI navigation
- Measurement equation and variables
- Hierarchical design
- Simulation setup
- Tuning and Optimization

Advanced Topics:

- Measurement-based model (MBM) creation
- Material property extraction
- Measurement-based model de-embedding
- S-Parameter Test Lab
- Interactive Data Display
- AEL Programming

TDR-01: TDR Basics - 0.5 Day

Instructor – Tom Dagostino

Prerequisites:

- Understanding of transmission line theory
- Experience with high speed (>10GHz) sampling oscilloscopes

Class Goals:

- What is TDR and how is it used?
- Understanding voltage, Zo and rho displayed information
- Basic understanding of the equations of TDR
- Limitations
  - Bandwidth
  - Losses
  - Resolution
  - Fixturing
- TDR vs. VNA Sxx display
- Trade-offs available to the user
- Conversion of TDR information into a usable model

TDR-02: TDR Based Modeling Using Tektronix' IConnect - 0.5 Day

Instructor – Tom Dagostino

Prerequisites:

- Understanding of transmission line theory
- Understanding of TDR technology
- Experience with high speed (>10GHz) sampling oscilloscopes

Class Goals:

- Transmission Line models
  - Lossless
  - Lossy
  - Single ended and differential
- Limitations
  - Bandwidth
  - Losses
  - Resolution
  - Fixturing
- S-parameter models
  - 2 and 4 port models
- How to improve models
- S-parameter Wizard
- Class demos

This class can be presented at customer's location or at Teraspeed Labs' office. At the office space is limited to 4 participants. On site a Tek TDR mainframe and TDR heads needs to be provided by the customer.

Instructors

Alfred P. Neves – Founder - Chief Technologist at WRT

Al teaches VNA, TDR, and channel modeling classes. Al is a Signal Integrity practitioner with over 30 years of experience in design and applications, and is one of the founders of WRT, and developed their physical layer and channel modeling platforms.

Ransom Stephens, Ph.D

Ransom teaches all jitter classes and helps engineers advance to technology's cutting edge. A pioneer in jitter analysis, he has served on the electrical working groups for several high data rate standards and has written over 300 articles, white papers, and application notes in the electronics industry.

Yuriy Shlepnev, Ph.D., Founder of Simberian Inc.

Yuriy teaches Advanced Electromagnetic Principles for Signal Integrity Engineers and is President and Founder of Simberian Inc., where he develops Simbeor electromagnetic signal integrity software. He received his Ph.D. degree in computational electromagnetics from Siberian State University of Telecommunications and Informatics in 1990. He was the principal developer of electromagnetic simulator for Eagleware Corporation and the leading developer of electromagnetic software for simulation of signal and power distribution networks at Mentor Graphics.

Chun-Ting "Tim" Wang Lee

Tim teaches advanced ADS training. He is a Ph.D student in the Electrical Engineering Department at the University of Colorado, Boulder, and is currently working part time for Wild River Technology on projects pertinent to PCB material property extraction and matching broadband measurements with simulation from kHz to GHz for signal integrity applications.

James C. Bell, Founder – Director of Design at WRT

James teaches Simbeor basics. He is one of the founders of Wild River Technology and is an experienced design and signal integrity engineer with over 30 years' experience in complex system design, interconnect, and signal integrity engineering. He has been a consultant to engineering organizations world-wide, with expertise in pre- and post-route signal integrity and timing validation foradvanced systems. He earned his B.S. in Electrical Engineering at Northern Arizona University.

Tom Dagostino, Owner of Teraspeed Labs

Tom founded Teraspeed Labs in 2002 to make measurement based IBIS Models and Signal Integrity related measurements for end customers. This is the continuation of his work that started in 1994 at Zeelan Technology and Mentor Graphics. In addition Tom supports the Tektronix IConnect TDR based modeling tool. Tom was also employed at Tektronix between 1974 and 1993 as a design engineer of digital oscilloscopes, project manager and performed market research and product planning in an inbound marketing position. Tom was awarded with 10 US patents during his early work developing digital oscilloscopes. Tom has also developed and taught classes on IBIS modeling and debugging, TDR technology and measurement based modeling techniques. Tom earned his BSEE from Worcester Polytechnic Institute.