Meeting the Demands of PAM4 Systems at 56Gbps and Beyond

Technology, a winning methodology and the desire to collaborate all matter

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Introduction

According to an IDC white paper sponsored by Seagate the global datasphere will grow from 33 zettabytes (one zettabye = one trillion gigabytes) in 2018 to 175 zettabytes by 2025. This white paper also reports that today, more than 5 billion consumers interact with data every day. By 2025, that number will be 6 billion, or 75 percent of the world's population. Figure 1 depicts this exponential growth. In 2025, each connected person will have at least one data interaction every 18 seconds. One last fact from this white paper: If you could download the entire 2025 global datasphere at an average of 25Mb/s, today's average connection speed across the United States, it would take one person 1.8 billion years to do it.

Clearly, there is a data explosion occurring with an ever-increasing requirement for dramatic bandwidth improvement to keep up. In this white paper, we'll explore some of the requirements to implement dramatic bandwidth improvements, Technology, methodology and strong collaboration all play a part.

Our discussion will focus on PAM4 (pulse amplitude modulation) systems operating at 56 Gigabits per second and beyond. PAM4 is a modulation technique whereby four distinct pulse amplitudes are used to convey the information. PAM4 enables twice the transmission capacity when compared to binary modulation. Because the additional voltage levels in PAM4 reduce the level spacing by a factor of three, PAM4 is more susceptible to noise than a binary digital signal, thus requiring a higher signal-to-noise (SNR) ratio. Consequently, PAM4 is normally used for short-reach applications where a higher SNR can be obtained.

We will explore how this shortcoming can be overcome, resulting in very long-reach signaling with PAM4 encoding over a copper cable to enable next-generation 25.6 and 51.2Tb/s switches, routers and 800G systems. Delivering this capability has two challenges — working silicon that can deliver the required performance and a SerDes test fixture that allows system designers to verify performance in their target application. We will discuss both challenges.

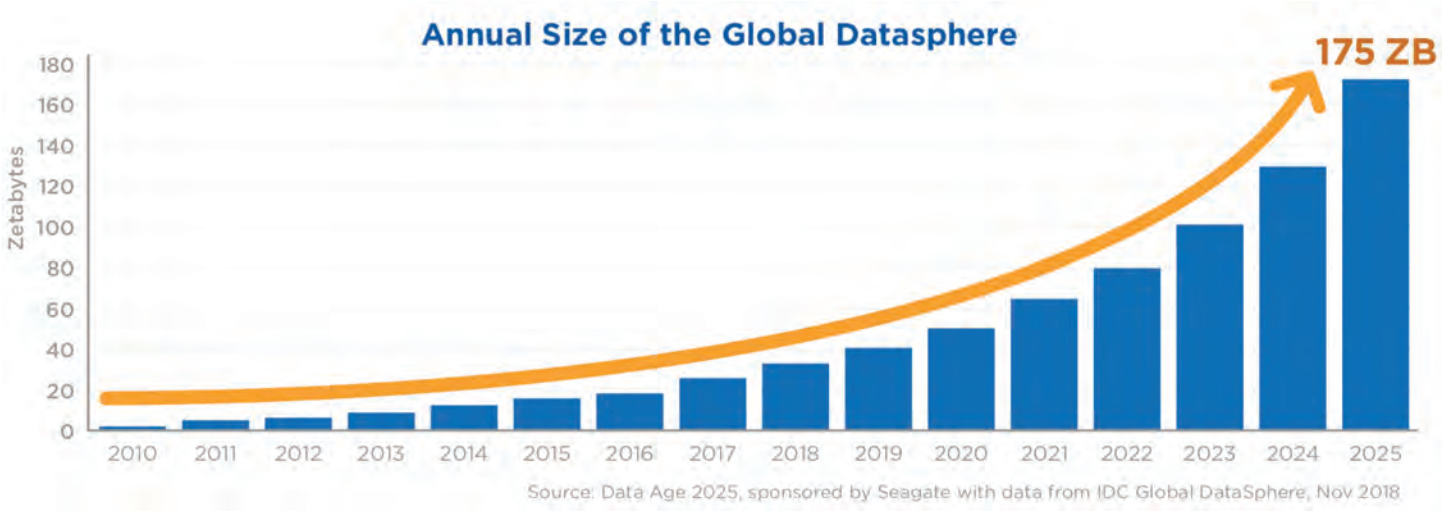

Figure 1. Exponential data growth

Design challenges

Regarding the silicon part of the solution, eSilicon has developed a full digital signal processing (DSP) (transmit and receive) 56Gbps SerDes in 7nm. A SerDes, or serializer/de-serializer, is a high-performance analog physical interface circuit that turns many parallel signals into a serial bitstream, transmits that bitstream over a physical link and then re-assembles the parallel data on the receiving end. Using this technique, large amounts of data can be transmitted over a small number of physical links, resulting in a more space-efficient design.

The eSilicon device delivers flexibility through a unique clocking architecture and firmware-controlled design. Thanks, in part, to a self-calibrated digital architecture with optimized power/performance trade-offs, the device can deliver true long-reach performance with very low power. The architecture is extensible to 112Gbps, which will be available later this year. The balance of this white paper will discuss the development of the test fixture for this SerDes.

The design challenge comes in two parts:

1. The ability to measure and electrically de-embed the fixture for compliance testing and characterization (we will define de-embedding below)
2. The ability to deliver the raw performance of the SerDes to the system interface with as little interference/loss as possible contributed by the test hardware

Signal and power integrity (SI/PI) are front and center in this type of design. Because of the high frequencies involved, the energy in the conductors essentially "leaks" to other conductors or ground planes. The goal of the SI/PI design team is to work out the design geometries in the region where the electrical and magnetic fields are not well behaved. Designing in this kind of environment requires enhanced, sophisticated analysis techniques.

Furthermore, the way these analysis techniques are applied is just as important. The designer needs to have an intuitive understanding of where the signal energy will go based on the physical design. S-parameter, or scatter parameter analysis, is helpful to model these types of effects. The skill required to perform this task demands a level of experience and insight that is frankly rare in our industry. World-class signal and power integrity engineers are "rock stars" in our ecosystem.

Beyond the actual design tasks, there is also a requirement for measurement. Measuring the actual performance of the physical SerDes test fixture provides one level of data. Another approach that enhances this analysis is a process called de-embedding. De-embedding uses a model of the SerDes test fixture and mathematically removes the fixture characteristics from the overall measurement, providing a "pure" model of the system without the physical effects contributed by the SerDes test fixture.

Achieving design excellence is often a subjective discussion. The good news here is that the IEEE is helping with the development of a formal specification. The IEEE P370 specification focuses on electrical characterization of printed circuit board and related interconnects at frequencies up to 50GHz. The P370 committee comprises approximately 60 members from 25 companies and universities. It has three task groups: Test Fixture Design Criteria, De-Embedding Verification, and S-Parameter Integrity and Validation. The design approaches described in this white paper utilize IEEE P370 for validation of results even though the design objectives extended to 70GHz, past the 50GHz addressed in the specification.

Exploring options

Wild River Technology performed the test system (i.e., test board) design. This organization consists of a team of the previously mentioned SI/PI "rock stars." The company's track record of successful delivery in high-speed design environments over many years was a key foundational element to our program.

The team explored signal power spectral density, examining how much bandwidth is needed for effective testing and what specific metrics of IEEE P370 are most important, such as return loss, equivalent return loss, time-domain reflectometry (TDR) and impedance analysis. It should be noted that, because of the advanced nature of this design, IBIS (input/output buffer information specification) models were not available, requiring an increased reliance on measured data. The design team evaluated many design options with speed and accuracy using measured data.

The core of the design was built around Samtec's Bulls Eye® Test Point System. This technology delivered an advanced cabling solution with performance to 50GHz and an efficient board footprint. The BE40A product was used for the current design. Collaboration was a critical element of this part of the program. Designing with high signal and power integrity requirements demands a tight interaction between the cable solution provider (Samtec) and the board designer (Wild River). Samtec understood how to support this effort, delivering complete and accurate models and a very high-quality test verification fixture that

was used to validate the signal integrity of the high-density Bulls Eye. This interaction between the teams provided the margin of victory for the project.

The methodology

The first version of the SerDes test fixture met many of the emerging IEEE P370 standard requirements. The ability to deliver a successful SerDes test fixture on the first pass is unusual for this type of high-performance design. A significant contributor to this success was the methodology employed. Three independent teams performed the signal integrity analysis — two at Wild River and one at Samtec. There was also a separate power integrity analysis team located at Wild River to ensure there were no troublesome resonances of the power planes impacting sensitive phased-locked loops (PLLs) and there was sufficient headroom to run all the digital data.

Each team performed an independent analysis and then the results were compared for consistency. Figure 2 illustrates the results of this comparison — a good correlation among the teams improved confidence in the design.

The idea for this process came from Alfred Neves, CTO at Wild River: "I got the idea for this approach from the early Apollo missions where they calculated launch trajectories with three teams working independently and concurrently. We all know this resulted in success for the Apollo program and it has resulted in success for our test system design as well."

To enhance the independence of the design teams, two different field solvers were used — ANSYS® HFSS™ and Simbeor THz.

The results

As discussed, the first version of the SerDes test fixture provided excellent working results. We have used this hardware at several high-profile events. Using Samtec ExaMAX® Backplane Connector paddle cards and a five-meter ExaMAX Backplane Cable Assembly, we are able to demonstrate true long-reach performance over a five-meter copper cable. Driving eight SerDes lanes, real-time data for voltage histograms (pre- and post-DSP), signal-to-noise ratio, equalization, eye diagrams and bit-error-rate plots are all available in real time to showcase industry-leading performance. Figure 3 illustrates the final SerDes test fixture and Figure 4 illustrates some of the real-time data presented at trade shows and technical conferences.

Mask (green dashed line) is based on PAM4 power spectral density and IEEE P370 quality metrics

3D EM Optimization Team Results

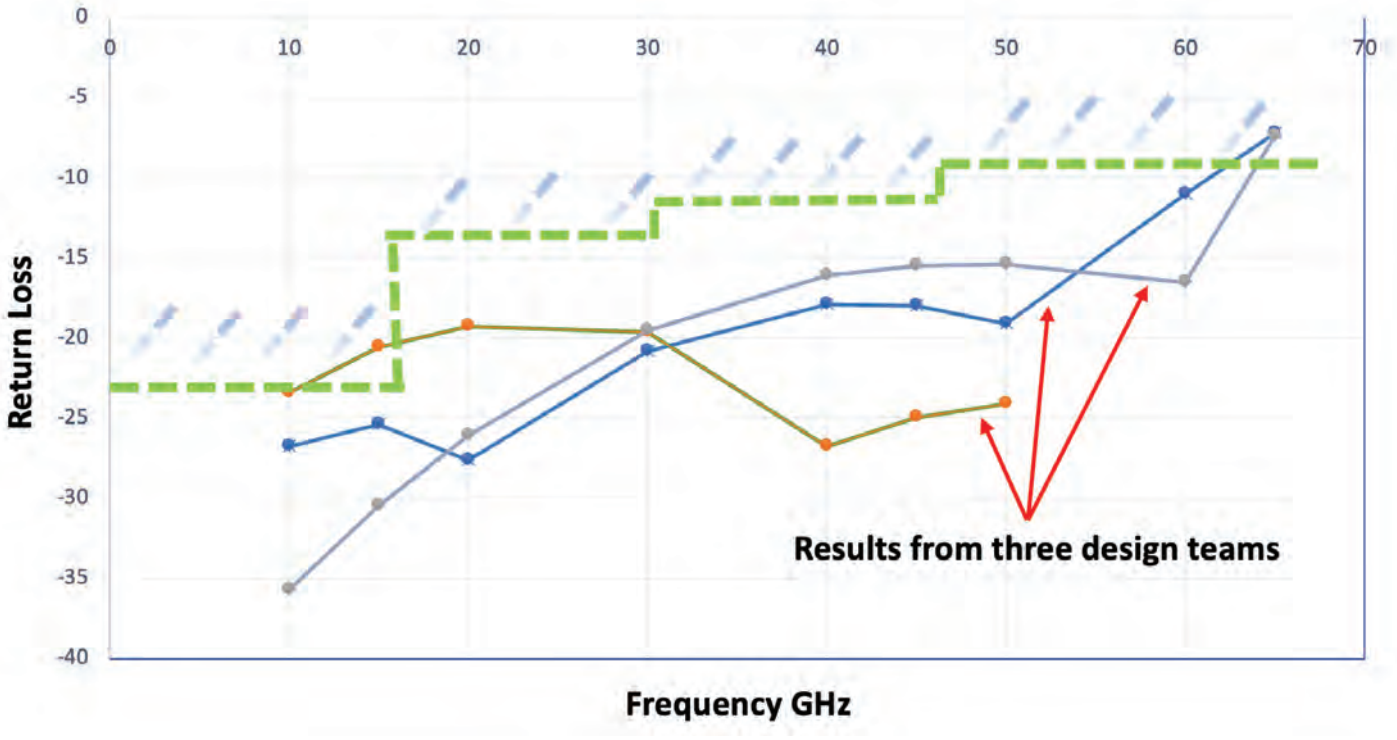

Figure 2. Independent SerDes test fixture design results comparison

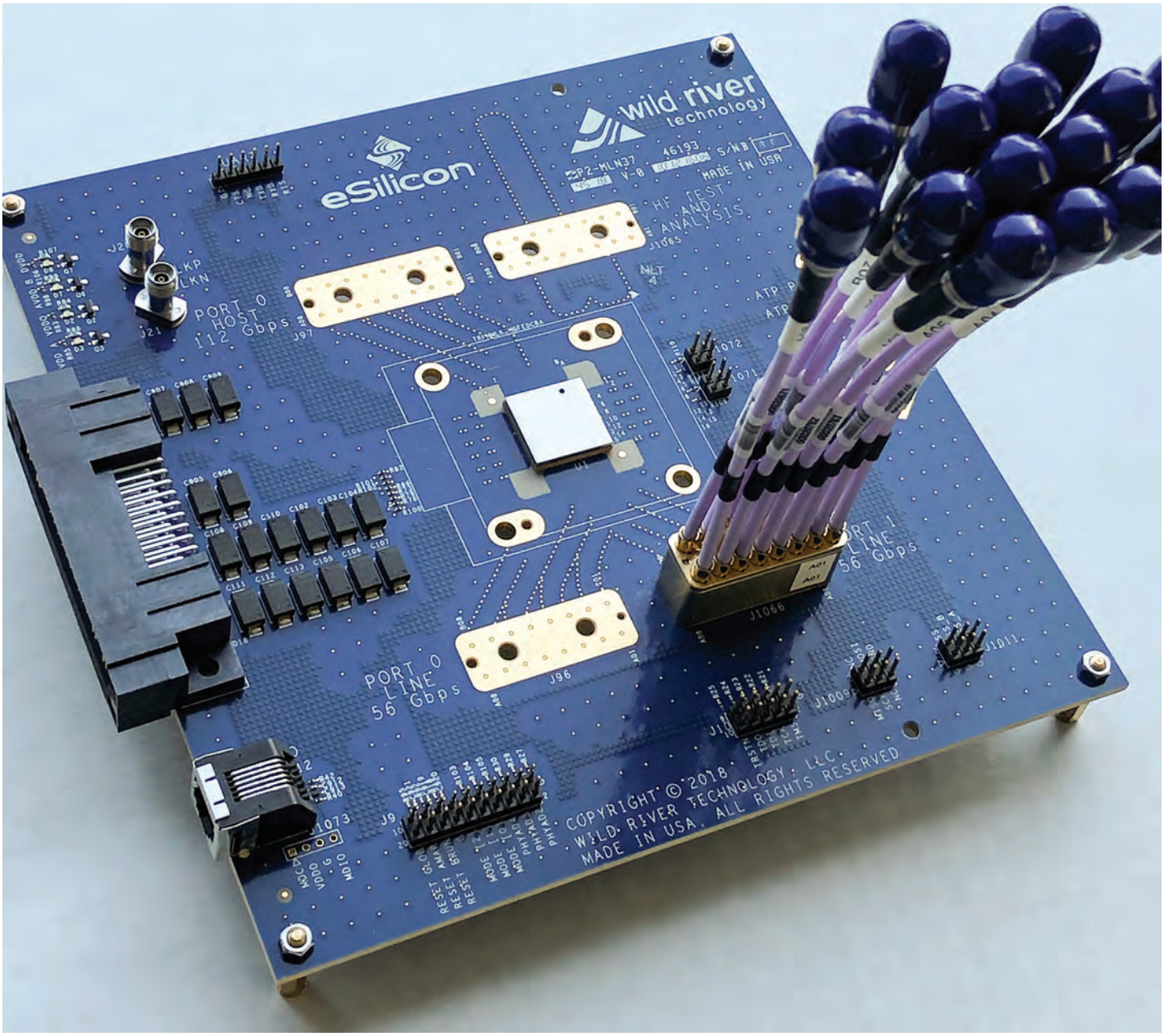

Figure 3. Final SerDes test fixture

Figure 4. Real-time SerDes test data display

An eye diagram is a common indicator of the quality of signals in high-speed digital transmissions. This display is constructed from a digital waveform by combining the parts of the waveform corresponding to each individual bit into a single graph. Figure 5 is a photo of such a display generated by the test fixture. Thanks to the clean data generated by this system we see a symmetrical display, the hallmark of an accurate channel.

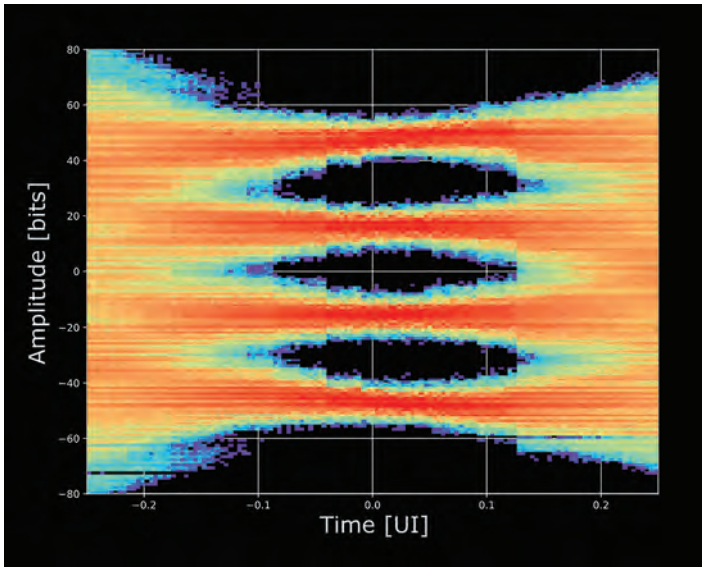

Figure 5. 56G long-reach full-DSP SerDes eye diagram display

What's next

A 112G version of the eSilicon SerDes will be available in the second half of 2019. This device will be implemented in 7nm technology and continue to deliver long-reach performance at very low power, supporting a wide array of highly flexible configurations.

A 70GHz version of the Bulls Eye Test Point System is currently under development. The high-density arrays replace traditional SubMiniature version A (SMA)-based layouts offering 4:1 space savings. This next-generation solution enables smaller evaluation boards and shorter trace lengths. Figure 6 illustrates the magnitude of the benefit.

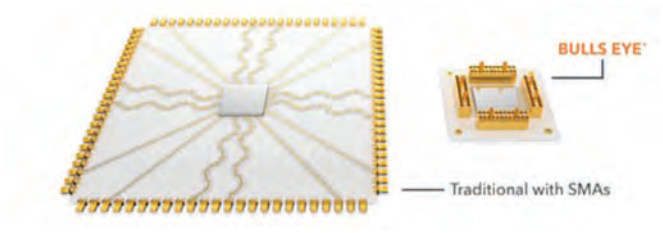

Figure 6. Space savings offered by the Bulls Eye System

Ultra-low-loss microwave cable contributes to improved performance. The compression interface eases PCB attachment and eliminates soldering costs. The Bulls Eye System also supports both microstrip or stripline PCB transmission types offering flexibility in signal routing. Additional high cycle count also contributes to make the Bulls Eye Test Point System ideal for high-performance test applications.

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