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Robust Method for Addressing 12 Gbps Interoperability for High-Loss and Crosstalk-Aggressed Channels

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Abstract
This paper addresses a new methodology for 12 Gbps interoperability that combines a concerted family of pathological channels, internal eye monitoring, and external EQ simulation tools, providing insight into an EQ optimization strategy that addresses the specific channel's mix of crosstalk noise, jitter, and channel loss. This also provides a backplane designer the ability to configure a high-loss, crosstalk aggressed system.

The method, combining co-simulation channel optimization, a reconfigurable channel platform, and receiver eye monitoring, has two key benefits; the separation of channel eye opening versus un-equalizable Deterministic Jitter (Dj), and the capability to map loss-crosstalk space for a particular SERDES channel pair, a new concept in SERDES interoperability evaluation.

The method is described in detail, followed by relevant case examples using hardware specifically designed for this endeavor. Finally, we compare eye monitor results with the original co-simulation, validating the method.

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Al Neves, Wild River Technology. Al has 30 years of experience in the design and application development of semiconductor products, capital equipment design focused on jitter and signal integrity analysis, and has successfully been involved with numerous business developments and startup activity for the last 13 years. Al focuses on measure-based model development, package characterization, high-speed board design, low jitter design, analysis, and training. He earned a B.S. in Applied Mathematics at the University of Massachusetts.

George Noh, Vitesse. George is a Technical Marketing Manager at Vitesse Semiconductor. He is the lead point-of-contact for new connectivity product definitions and involved in roadmap and early stage development phases with early access alpha customers. He has had involvement

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I. Introduction

One of the most notable landmarks to the establishment of the discipline of information theory was the publication of Claude E. Shannon's classic paper "A Mathematical Theory of Communication" in 1948. The essential principal is that both limited bandwidth and noise limit a channels capacity for information throughput. Today, as data rates continue upward, crosstalk-generated energy versus channel losses echo the issues addressed back then, especially when considering data rates exceeding 10 Gbpsec encounter closed eyes.

In 10 Gbpsec or faster systems, noise is coupled into the channel to form crosstalk and, after adding the impact of channel loss or Intersymbol Interference (ISI), the eye as seen by the receiver is often almost totally closed. Traditional jitter analysis methodology requires at least some eye opening to establish any meaning, so former methods are not that helpful. Equalization is required to "whiten" the channel's net signal loss, thereby opening the eye, but this often aggravates the crosstalk impact or other forms of Random Jitter (Rj).

Activities and methodologies engineers pursue for 12 Gbpsec+ interoperability often include:

- Compliance specific plug-fests
- Corner-case channel implementation
- Search for a normative channel
- Zero length THRU in conjunction with TCTF test structures
- Statistical simulation using Stat-Eye type tools or other convolutional type simulators
- Test on a large number of platforms related to specific compliance specifications

Often, even after some measure of EQ, the desired BER performance is still not achieved in many channels. Some system elements have interoperability issues while others work very well after EQ is optimized for the given channel. Still others have SERDES with high Bit Error Rate (BER) with the given channel. The situation is clearly a bit of a mess, and there is no clear tractable methodology that addresses the full scope of the problem. In the best case, where the channel achieves good BER, it is not always clear what margin exists as it is usually not possible to examine the opened eye inside the receiver.

Take the example shown in Figure 1 and Figure 2 of a TCTF SFP+ Compliance Channel using 3 inch and 11 inch differential stripline traces. Matched low skew cables were used to connect the two structures together. In Figure 1 the TCTF mask is juxtaposed to measured S-parameters, illustrating compliance. Figure 2 shows the corresponding eye to be almost closed.

One benefit of the Method about to be discussed is that it will answer the question "Can a particular SERDES architecture recover data from the stressed eye shown in Figure 2?".

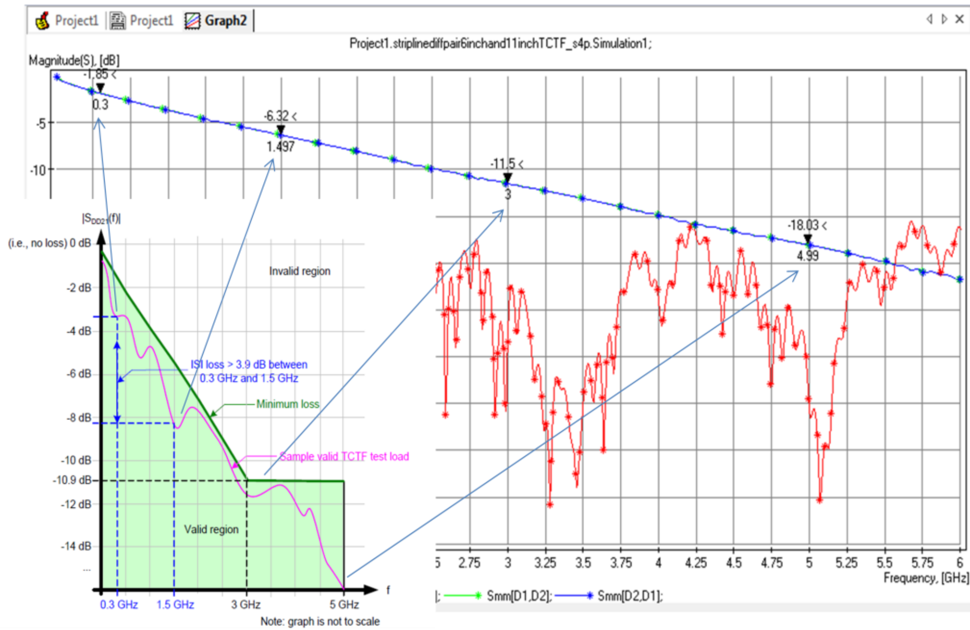

Figure 1 - Example of TCTF SFP+ Compliance Channel using a combination of 3inch and 11inch Differential Stripline traces

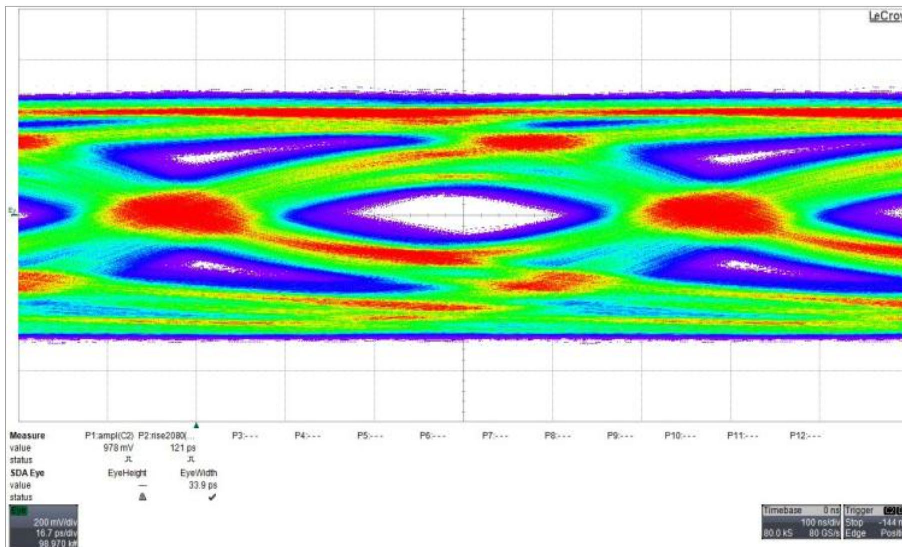

Figure 2 – Graph of the TCTF SFP+ Compliance Channel stressed eye pattern

This paper addresses a new methodology that combines a family of pathological channels (in the form of a channel modeling platform PCB), internal eye monitoring, and external simulation tools, providing insight into a EQ optimization strategy that addresses a specific channel's mix of crosstalk noise and jitter, and loss in the channel. This powerful methodology of using pre-defined channel modeling platform test structures, RX internal eye monitoring, and external EQ emulation simulation capability also provides the ability for the high-speed backplane designer to configure a high-loss, crosstalk aggressed system without designing any backplane type hardware.

The Method, Step by Step

Step 1 of the Method involves creating a **concerted library of S-parameter models** of both post-layout measured channels and pre-layout modeled channels – *prior to implementing a specific SERDES solution*. The pre-layout s-parameters can also be created by assembling prior s-parameter models and chaining them together for a new net model, one purely created by 3D EM solver tools [2]. In the case of silicon vendors, channels representative of customer backplanes could obviously be included in the form of S-parameter models. For the actual measured cases (backplanes, channel model platforms, customer specific channels, line cards, etc.) we will briefly illustrate our metrology testing for passivity/causality and any related symmetries in the multi-port measurement, along with requirements for sampling interval and bandwidth suited for 12 Gbpsec data rates.

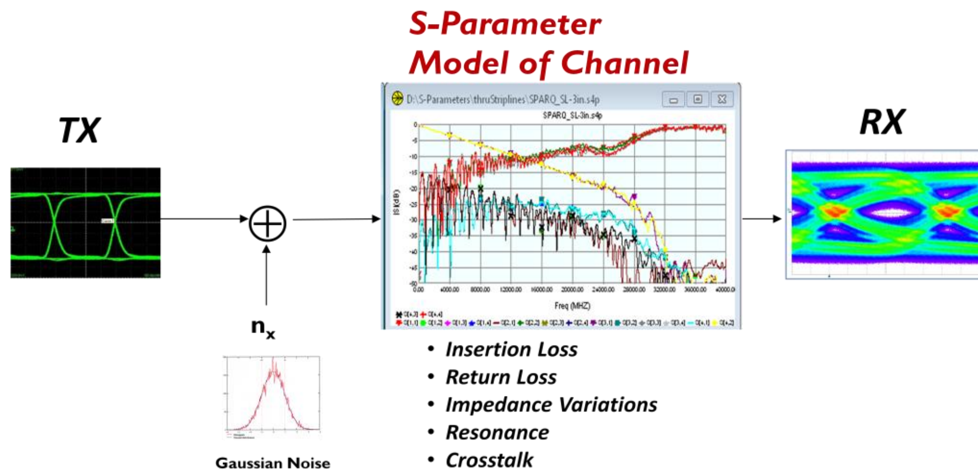

Figure 3 - The Method involves using a host of channel models and a perfect TX/RX (no RJ so n_x=0)

Step 2 of the Method involves first using a host of channel models and a perfect TX/RX (no RJ) (see Figure 3) using software emulation, then using actual Silicon channel of TX/RX where the post equalized eye is monitored. This involves a combination of **virtual probing and equalizer emulation** using either a software tool developed by LeCroy, called SI-Studio, or alternatively MATLAB® or Agilent ADS to perform this same simulation. This step utilizes EQ emulation, which uses an s-parameter model (provided by the library mentioned in Step 1), linear FFE, DFE filters, and clock recovery to create a simple RX model. The user must provide a system description file of their circuit elements and Touchstone formatted s-parameters. This equalized receiver therefore forms the basis for a software-defined reference EQ receiver. Importantly, this step evaluates the channel with either your own FFE, DFE filter architecture, or one defined by existing silicon, without introducing tolerance RX issues or TX jitter, DCD, or DDJ. This step also serves to separate the silicon issues from the channels issues. If software emulation cannot derive a suitably satisfactory EQ response, certainly actual silicon with jitter and tolerance issues will not either. This step also addresses suitable topologies early in the full link design process.

This step first involves spectrum of clean loss channels either with direct measurements or extracted s-parameters from scalable transmission line models (RLCG, W-element, etc.). "Clean" specifically refers to channels that have decent return loss several factors past the

Nyquist sampling data rate, and includes structures that are both short and low loss and long with enough loss and subsequent ISI to almost close the eye at a given data rate. It is important to isolate the impact of loss, not reflections, resonances, and other pathology due to poor return loss. There is no XTLK aggression energy related to this step. Importantly, the recovered waveform, as simulated by the s-parameter model and EQ emulation in the Virtual Probe software, is sampled at the Slicer, which is internal to the RX silicon. This makes the method consistent with Step 4 below, where we compare to actual silicon. Alternatives of adding RX equalization or TX driver pre-emphasis to an optimized DFE tap number would be addressed in this step as well.

The second part of step 3 includes channels with pathology: poor return loss, reflections in the channel due to VIA fields, poor TX and RX termination, suck outs in response, resonance as you would find in poorly laid out connectors, modal conversions, etc., While the first part deals with clean channels with classic ISI due to loss, the second part deals with multiple reflections in the channel requiring careful optimization of the TX/RX CTLE, DFE, and FFE filters.

Step 3 of the Method compares the Virtual Probe emulation results to actual silicon measurement using internal eye monitoring. No crosstalk is aggressed at this point (the aggressors are simply terminated); this is a correspondence check between internal eye monitor and perfect TX/RX in the EDA emulation. Both virtual and silicon probing involve sampling the eye at the critical BER monitor point. We will explain why a full comparison benchmarking differences between actual silicon and virtual probing should be done and the benefits of creating a full library of optimized pathological channels measured from an agile channel model platform. We will also explain why it is preferable to use a low jitter BERT for TX and then add TX of actual silicon to de-embed the impact of TX random jitter, DDJ, and DCD.

In Step 4 of the Method increased levels of crosstalk aggression are added to a suitable group of channels on the channel model platform, then re-optimizing their channel response for BER. The channel will be re-optimized at this step. It is important to use the same pathological structures used in Step 3 and in Step 5 as well.

Step 5 of the Method maps the full Crosstalk-Loss space for both 10^{-12} BER and gross Clock & Data Recovery (CDR) locking capability. The Crosstalk-Loss space represents a new approach to RX tolerance which includes impact of channel, SERDES pair, and specific EQ optimization. A case example is included later in the paper, illustrating the full method using an Agilent JBERT, a suitable channel modeling platform, Centellax data generators, and a Vitesse SERDES device [12-15].

II. The Channel Modeling Concept and S-Parameter Data Mined Libraries

Step 1 of the methodology is the creation of a comprehensive set of S-parameter channel models, an essential element [2]. These models can be created by:

- 3D-EM synthesized S-parameters
- S-parameters from Rational Compact Model Simulations

- Customer specified VNA measurements (backplanes, test platforms, etc.,,)
- TDNA measurements (time domain approached frequency domain, example includes SPARQ, IConnect)

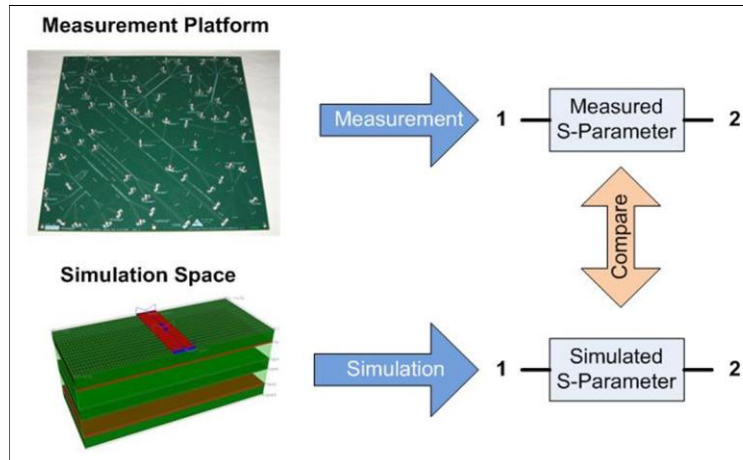

Figure 4 - Measurement versus Simulation Space Comparison

A key issue related to this concept is creating a comprehensive library of passive/causal and validated S-parameters derived from either VNA or TDNA methods. They are then compared to simulation results using well understood material properties in the platform and good loss models (See Figure 4). This process validates both simulation and measurement spaces.

Channel Modeling Platform Description

The physical layer reference design platform we utilized is shown in Figure 5 and is designed to provide a set of structures to identify parameters of low-cost FR-4 dielectric and to benchmark electromagnetic analysis software with measurements. All test structures are equipped with well optimized launches from SMA connectors to micro-strip lines. SMA connectors are used instead of probes to make all measurements repeatable and to use the board for methodological and pedagogical purposes.

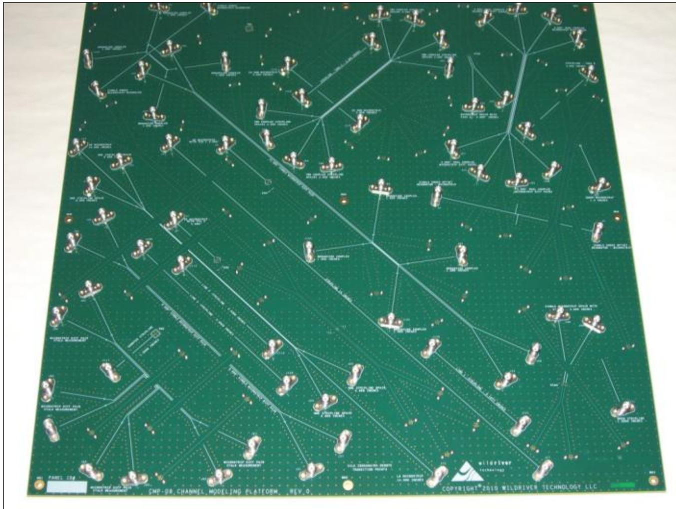

Figure 5 – CMP-08 4th generation Channel Modeling Platform

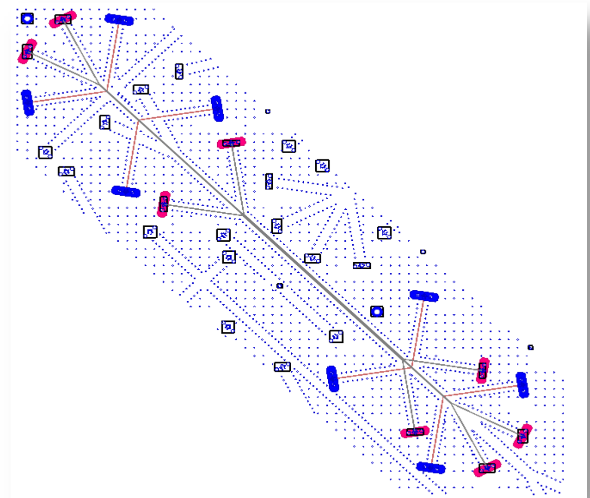

Figure 6 - Broadside/Coplanar Coupled Structure

(a)
STRIPLINE DPAIR
L4 3.000 INCHES

(b)
STRIPLINE DPAIR
L4 6.000 INCHES

(c)
STRIPLINE DPAIR
L5 11.000 INCHES

(d)
J90
J91
J94
J95
J96
J92
J93
J97
STRIPLINE DPAIR
L4 11.000 INCHES
Rx
Tx
COPLANER COUPLED
DPAIR 5.000 INCHES
J98
J102
J103
J99
J100
J101
J104
J105
BROADSIDE COUPLED
DPAIR L5 1.00 INCHES
BROADSIDE COUPLED
DPAIR L5 1.00 INCHES

Figure 7 – Test structures used in this paper. a) Stripline differential pair, 3 inches. b.) Stripline differential pair, 6 inches. c.) Stripline differential pair, 11 inches. d.) Stripline differential pair, 11 inches, coplanar and broadside coupled

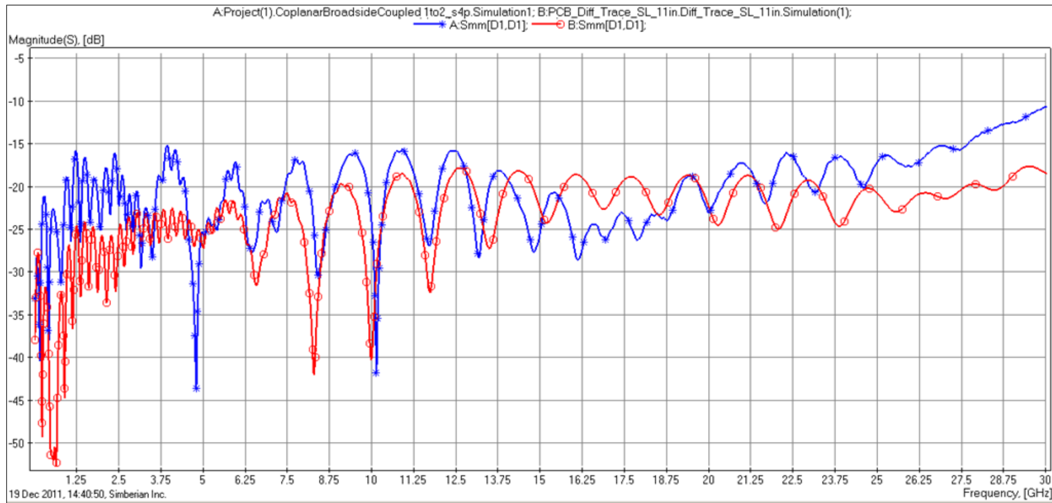

Figure 8 - Return loss comparison of simple 11 inch stripline differential pair (red) to 11 inch stripline differential pair with 1 inch of broadside coupling (blue) with passive aggressors

The Broadside Coplanar structure in Figure 7(d) consists of an 11inch stripline differential pair with 3 sets of coupling structures. Differential Return loss (SDD21, see Figure 8) is comparable to a simple 11inch stripline differential pair (with no crosstalk coupling structures), but the Broadside- Coplanar coupled structure shows high modal common-mode to differential conversion (SDC21).

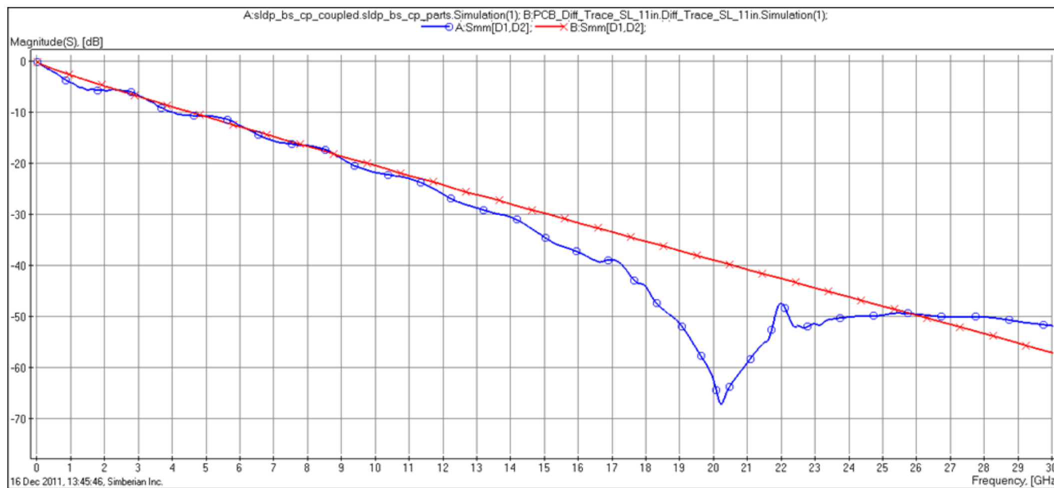

Figure 9 - Insertion loss comparison of simple 11 inch stripline differential pair (red) to 11 inch stripline differential pair with 1 inch of broadside coupling (blue)

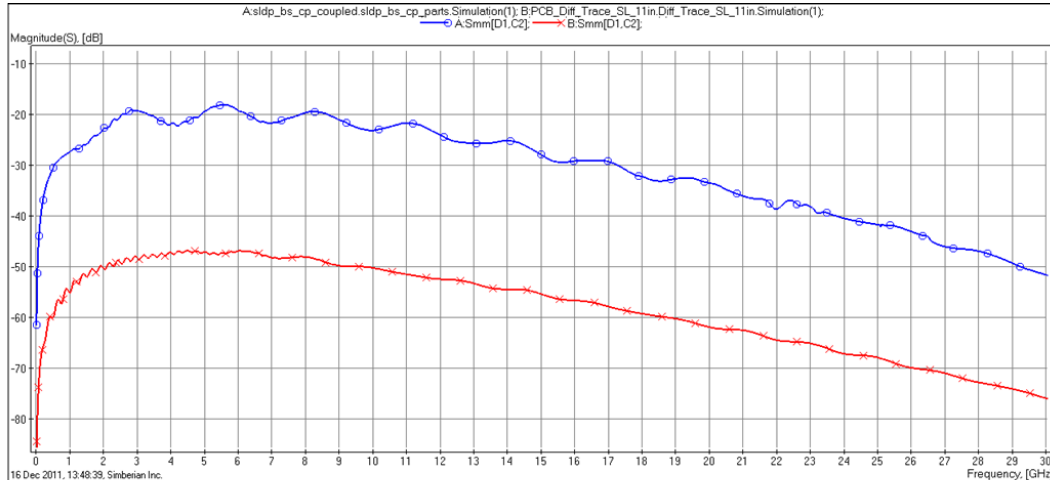

Figure 10 – Mode Conversion (Common-Mode to Differential) comparison of simple 11 inch stripline differential pair (red) to 11 inch stripline differential pair with 1 inch of broadside coupling (blue)

The following describes the rational for design and characteristics of the broadside-coplanar structure. Typical backplane and midplane based interconnect channels include multiple line cards attached to an interconnect board through electrically large connectors. Crosstalk isolation in high speed connectors has improved in recent years, but there are always opportunities for neighboring aggressive nets to induce crosstalk into a victim through coupled routing within the connector breakout region, within the connector, and within the via breakout fields. These sections are often relatively short, with lengths less than 1 inch, but can often have high coupling coefficients. Within each connector field there can be as many as 8 nearest neighbor aggressors, comprising the 8 differential signals surrounding a connector in the adjacent rows and columns. In addition, there may be two same layer aggressors on the midplane on either side of a victim trace.

It is generally not feasible to instrument 8 aggressors on each end of midplane, along with two aggressors on either side of a victim, in a small compact structure that is both easy to measure and to model. However, it is possible to emulate the equivalent of several strong aggressors in three places along the interconnect: at the equivalent of the Tx side connector, at the Rx side connector equivalent, and in the backplane trace routing section between the two connectors. The Broadside and Coplanar Coupled test structure (Figure 7d was designed for this purpose; simplified evaluation of real interconnect cases with the inclusion of complex crosstalk induced DDJ.

In the Broadside and Coplanar Coupled Structure, an 11 inch long differential stripline is coupled into a one inch long broadside differential pair with a high coupling coefficient of $> 20\%$, a value of coupling high enough to induce the equivalent crosstalk typical for worst case correlated aggressors. Tx aggressor drivers can be placed preferentially on the near end side of the coupler to simulate Tx-to-Tx same direction crosstalk, or on the far end side to simulate Tx-to Tx opposite direction crosstalk. This second type of crosstalk can create significant far end crosstalk at the receiver. A duplicate broadside coupler is also placed at the far end receiver side of the 11 inch long victim, to simulate additional crosstalk on the receiver side. Again, aggressor Tx port placement can be used to simulate Tx transitioning in the same direction as the Rx

received waveform, which is the most favorable configuration, or in the opposite direction, which causes maximum received crosstalk.

Offset from the center of the victim pair is a 5 inch long coupled differential aggressor on the same stripline layer, split to surround the victim on each side. This side-to-slide split provides a 2X amplification of the injected differential mode crosstalk, as seen by the victim. The center coupled section is designed to have asymmetric placement, directly adjacent to the broadside coupler on one side of the interconnect, and about 3 inches away from the coupler on the other side. Because no effort was made to adjust victim characteristic impedance in the coupled section, the offset placement of each coupled section presents a complex impedance reflection profile to the interconnect, along with complex superposition of the crosstalk waveforms injected into the victim channel. These channel complexities are, however, designed to be easily modeled with commercial full wave electromagnetic solvers, and measured with conventional time and frequency domain instruments.

Dielectric and Conductor Surface Roughness Identification

We adopted a simple but accurate method of modeling loss in the channel. Dielectric and conductor roughness parameters are identified with generalized modal S-parameters (GMS-parameters) technique. This simple and practical procedure was first proposed in [1], validated on different materials in [2]-[5], and implemented in Simbeor software [6] that was used here to identify material models. The material identification method is based on comparison of the GMS-parameters extracted from the measured data with GMS-parameters computed for a line segment without launches or connectors. The key in such comparison is the minimal number or the parameters to match. Only generalized modal transmission parameters are not zero and are used for identification. Both computed and measured generalized reflection and modal transition parameters are equal to zero exactly. It simplifies the identification process a lot without sacrificing the accuracy and makes the GMS-parameters method the simplest possible. It does not require multiple structures for broad-band TRL calibration and expensive 3D full-wave modeling of launches and connectors. S-parameters measured for two segments of line of any type and with any characteristic impedance and launches can be used to identify material properties. Here we used GMS-parameters of coupled lines for identification of material properties for layered and anisotropic dielectrics. We identified material models by matching phase or group delay and magnitude for generalized even and odd mode transmission parameters. The models were suitable for accurate simulation of multi-gigabit signals in differential and coupled interconnects. Identified dielectric models were validated with the measurements for different coupled differential structures.

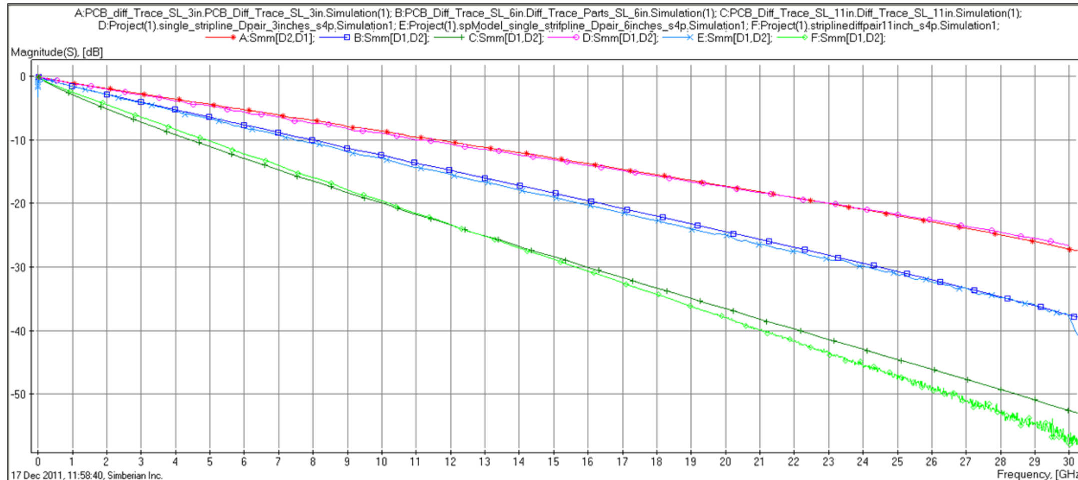

Figure 11 - Correspondence of SDD21, Differential Insertion loss of 3, 6, and 11 inch Stripline structure from simulation to measurement which confirms stellar loss modeling after dielectric and conductor roughness parameters were identified.

Analysis of S-Parameters, i.e., "Data Mining"

The 4-port S-parameter measurements of a differential channel provide a complete electrical description of the behavior of the channel. This data is often referred to as a black-box behavioral model in that it can be used in a circuit simulation without ever opening the box to see what is inside.

However, immediate insight can be gained about the general properties of the interconnect by performing a few simple observations. In particular, five parameters are of particular interest: the differential insertion and return loss, the differential and common time delay, and the mode conversion terms.

If you want to have a favorite S-parameter term, it should be the differential insertion loss. This term is the ratio of the received differential signal to the incident differential signal. It most directly describes the channel as seen by differential signals. At a glance, the differential insertion loss, SDD21, identifies the bandwidths of the channel, as defined by the -3 dB point, the -10 dB point, or the -20 dB point.

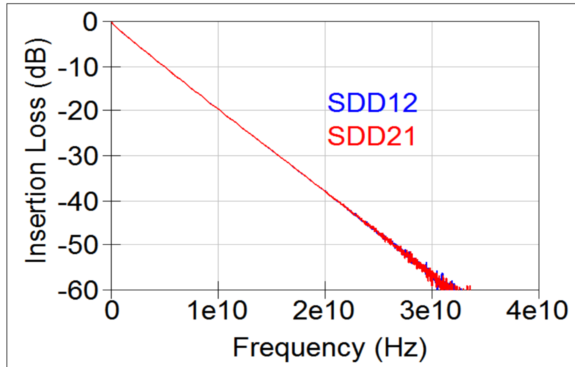

Figure 12 – Insertion loss of the example channel

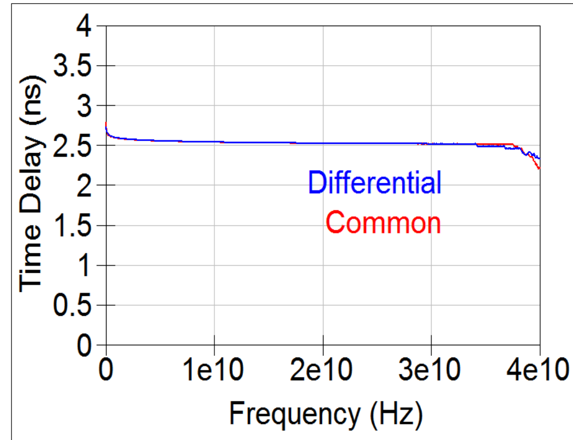

Figure 13 - Plot of Channel Time Delay

In the example shown in Figure 12, the -10 dB bandwidth is 5 GHz, suggesting that if the received signal requires at least -10 dB of amplitude, the highest data rate without equalization might be 10 Gbps. The slope of the insertion loss is 2 dB/GHz.

From the slope of the insertion loss and the length of the channel the normalized insertion loss, a useful figure of merit, can be easily calculated as about 2 dB/GHz/11inches = 0.18 dB/in/GHz. From just the dielectric loss in FR4, the expected normalized loss is about 0.1 dB/inch/GHz. This suggests a contribution of higher dissipation factor in the channel laminate and some conductor loss as well.

It's always a good policy to check that SDD21 = SDD12. Reciprocity is a property of all linear passive systems. If this condition is not met, it is usually an indication of a problem with the data such as poor calibration or connections.

The phase of the insertion loss has information about the time delay of the channel. The total number of cycles divided by the frequency is a direct measure of the time delay. In this channel, the time delay of the differential signal, above about 1 GHz is 2.5 nsec. Below 1 GHz, there is slight frequency dependence, an indication of dispersion in the material, which is expected in most polymer materials.

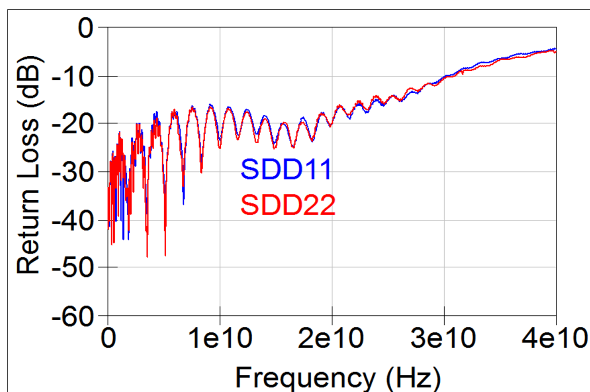

Figure 14 – Plot of Return Loss

The time delay difference between the differential signal and the common signal is a measure of the difference in overlap between the even mode and odd mode electric fields and the dielectric materials. In homogenous channels, or uncoupled differential pairs, the differential and common delays should be the same. This is a useful consistency check.

Return loss is a very sensitive measure of the impedance profile of the channel. While there is no spatial information in the frequency domain

display of the return loss, it's possible to identify some interconnect features from the return loss patterns. The ripple in the insertion loss is due to either the line impedance mismatch from the port impedance, or discontinuities at the ends of the line from the launches. The fact that the return loss increases above 20 GHz is usually an indication of reflections from the launches. The

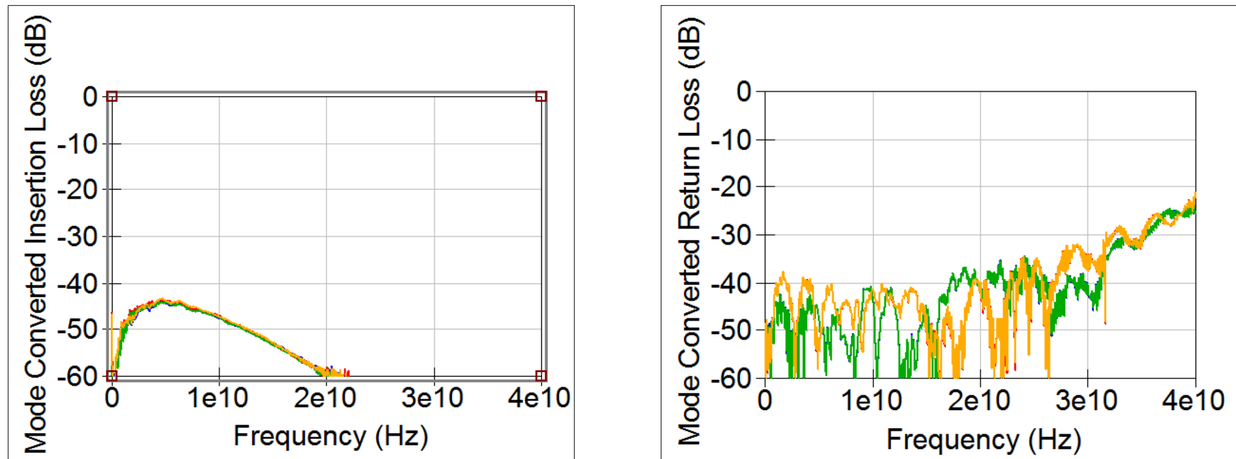

Figure 15 - Plots of channel mode conversion in insertion and return loss

impedance of the via pad stack under the SMA generally increases with frequency.

Finally, mode conversion in the channel can be evaluated at a glance of the SCD and SDC terms. Mode conversion only results from an asymmetry between the two lines that make up the pair. While mode conversion will distort the differential signal, there are other consequences. In this example, the mode conversion is less than -35 dB up to 30 GHz, which indicates excellent symmetry in the channel.

To use the S-parameter measurements as a behavioral model does not require opening the lid, but as illustrated above, some insight into channel performance expectations can be gained by analyzing the measured data.

Practical S-parameter Integrity

As was discussed earlier, the starting point for this method is establishing a comprehensive S-parameter library encompassing a wide swath of channels, some normative, others highly pathological (modal conversions, resonance lasting many UI bit periods, wrong impedance objectives, etc.). And, considering this library will consist of backplanes, channel modeling platform test structure, customer measurements, compliance masked defined S-parameters, whatever… it is important to insure the integrity of the S-parameters by maintaining a clear process of S-parameter checking [20,21,25].

The purpose of this section is to provide a quick method of assessing S-parameter integrity of any give measured S-parameter [22]. It is not exhaustive, it is not empirical, and much of it is based on the experience of the authors, but it is cook book oriented and addresses a plethora of practical measurement issues.

It is important to develop an evolving metrology verification approach that you have confidence in, and that confidence is based on experience and any new measurement requirements.

The first question that should be asked upon receipt of S-parameters should include: How was the VNA or TDNA calibrated, and where are the validation measurements? Validation (as discussed later) includes use of known structures like singled-ended or differential THRU's, 25 and 50ohm airlines, on-board substrates, wideband 50ohm loads, T-checkers, etc., identifying both the type of calibration, validation of the calibration via measurement and some thinking about what errors are relevant. For example E_{tf}, or Forward Transmission Error, is very important for short low loss structures with very low return loss. An example of this is simply measuring a KF-KF (female-female connector) adapter between cable pairs when the cable ends are male-male (ends of the cables represent a SOLT-calibrated reference plane).

It is important to establish a corresponding bandwidth requirement that is typically based on Nyquist for a give data rate, such that a 10 Gbpsec NRZ data pattern has a corresponding 5 GHz Nyquist frequency. This frequency is significant in that most of the power spectral density of the NRZ signal is less than 5 GHz. Measurement objectives for 10 Gbpsec is often (this is debatable) for 5x Nyquist, or 25 GHz for reasonable jitter modeling correspondence. Typically, a minimum stop frequency of 40 GHz is employed, this being based on experience, opinion, and desire to margin the measurement. Numerous references discuss time domain causality issues from inadequate measurement bandwidth.

Bandwidth (or BW per data rate) requirements dictate:

- Fixture Architecture and Design –
    - Do my measurement fixtures provide adequate return loss (SDD11) to desired frequency?
    - Does the fixture incorporate adequate calibration structures?
    - Does the calibration for VNA or TNDA match the bandwidth, etc.?
- VNA, PNA, TDNA selection
- Calibration approach that provides desired minimal residual calibration error at 5X Nyquist frequency for a given data rate
- BERT data rate (for correspondence between eye measurements and simulated)
- Cabling, adapters, connector kits (for example, 40GHz is the limit Fstop for K connectorized fixtures since calibration kits for K connectors are limited to 40GHz BW)

Preparing for measurements, the first step is to check basic sampling points and set start and stop frequencies. Our settings: 40 GHz Stop Frequency, >1601 points (more points for longer structures), reasonably low VNA IF bandwidths (we use 500Hz as a practical compromise of sweep time versus noise tradeoffs). The Start or minimum frequency is dictated by the full electrical length of the structures, and therefore includes reflections in the channel. In most applications 10 MHz - 25 MHz is a sufficient Fstart for 10 Gbpsec with practical signal lengths

less than 6 nsec in electrical length.   Other practice includes a small IF bandwidth of 500Hz, and averages of 8 waveforms.

Secondly, we typically plot the full S-parameter matrix (all 16 for 4 ports for example) of our desired Channel set up to validate the measurement approach. We typically check for gross problems such as obvious passivity, significant group delay distortion, etc. A key focus at this step is analysis of return loss quality. The objective is to maintain a maximum of -17dB out to at least 3x Nyquist frequencies (rule of thumb, again opinion and our experience).

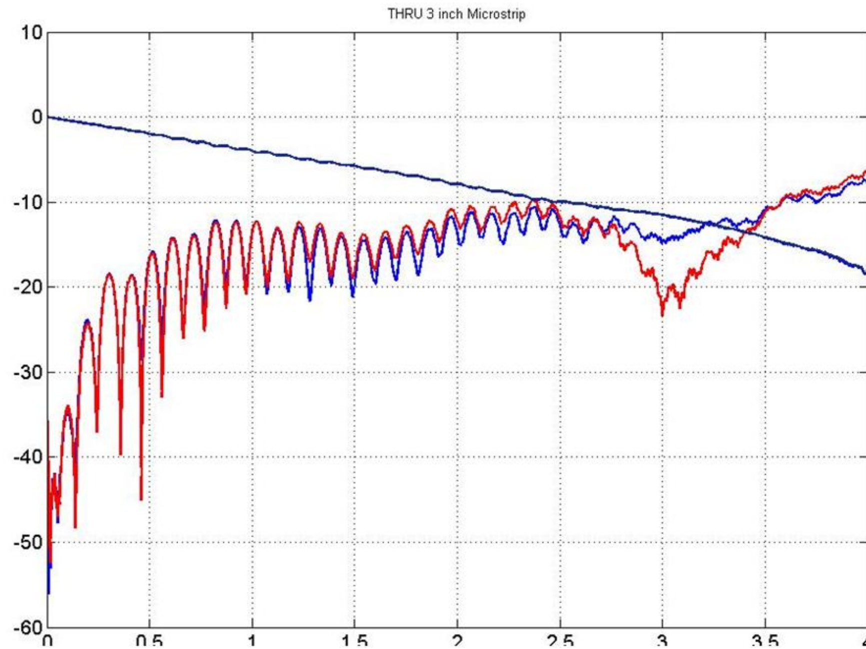

Figure 16 – Loss graph of 3 inch single-ended THRU with poor S11, S22.

A practical example regarding return loss: Short, low-loss, and low reflectance structures are good starting points to validate measurement setups. A simple 3 inch single-ended THRU seems simple, yet upon close inspection of the S2P measurement s11 we see evidence of ripple in insertion loss (dark blue) due to poor return loss of -14dB less than 1GHz.   In this case the launch vias were not fabricated correctly due to an incorrect drill hole size used for signal via fabrication making the via high excess capacitive.

For all marginally poor SI devices such as this THRU, we typically find it very valuable to perform TDNA analysis either using VNA and time domain gating, or direct TDR, TDT measurements (see Figure 17).   It helps with assigning return loss issues topologically in the test fixture.

Figure 17 - Example of TDNA method for THRU fixture evaluation where both passive and causal time and frequency domain plots are conveniently available on one plot. This provides immediate topological mapping from structure issues to S-parameter degradation. Left plot is differential mode, right plot is common mode response.

A second example (Figure 18) is a 4-port that extends the THRU from single-ended to a differential structure, performing a quick S-parameter check of all 16 S-parameters in the full 4-port system (Figure 19). The check for 4 ports we then examine return loss, symmetry (s11=s22, s33=s44, etc.,) and reciprocity (s21=s12, s34=s43, etc.,) as well as magnitude of all return losses. Not discussed specifically, the next step would include multi-mode check of SDD21, SDD11, and SDC21 for mode conversion issues due to weave, skew, non-homogenous materials, etc.

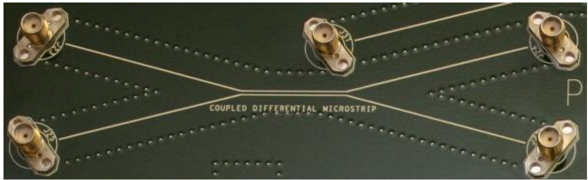

Figure 18 - A simple 3 inch Differential THRU

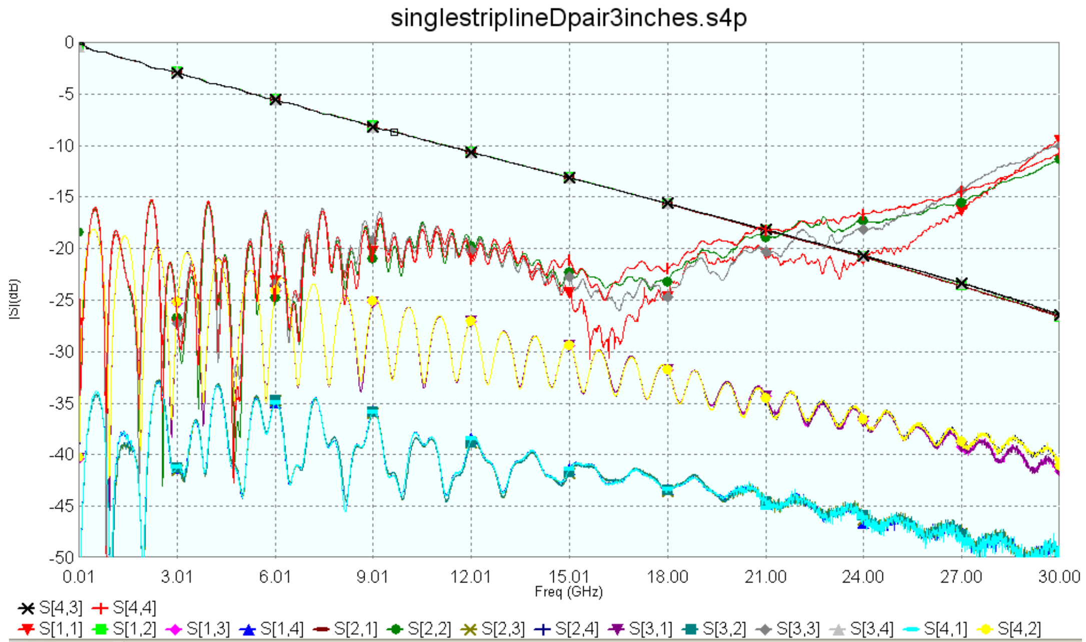

Figure 19 - 16 S-parameters of Differential 3 inch THRU

Structures that are symmetric and have good connector repeatability will be by definition symmetric (see Figure 20).

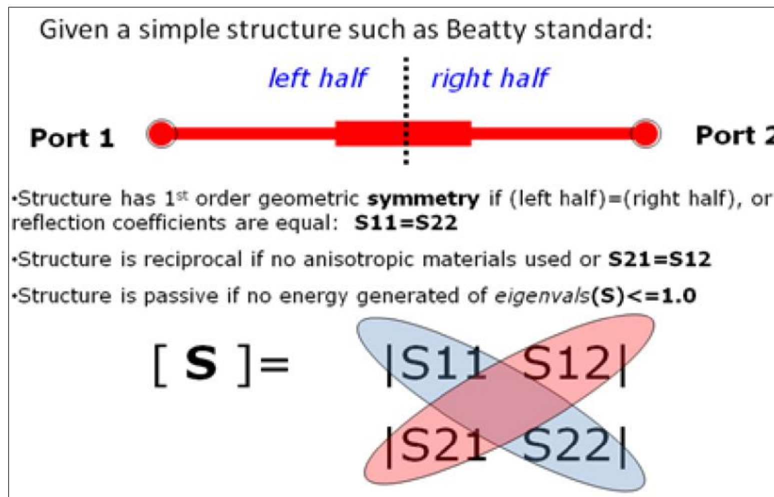

Figure 20 - Symmetry and Reciprocity vs. Structure

The plot shown in Figure 21 below illustrates good symmetry between s11 and s22, which should be expected for symmetric structures like the 80ohm Beatty Standard (included on CMP-08 Platform). The black line shows the symmetry magnitude error is reasonably low out to 30GHz.

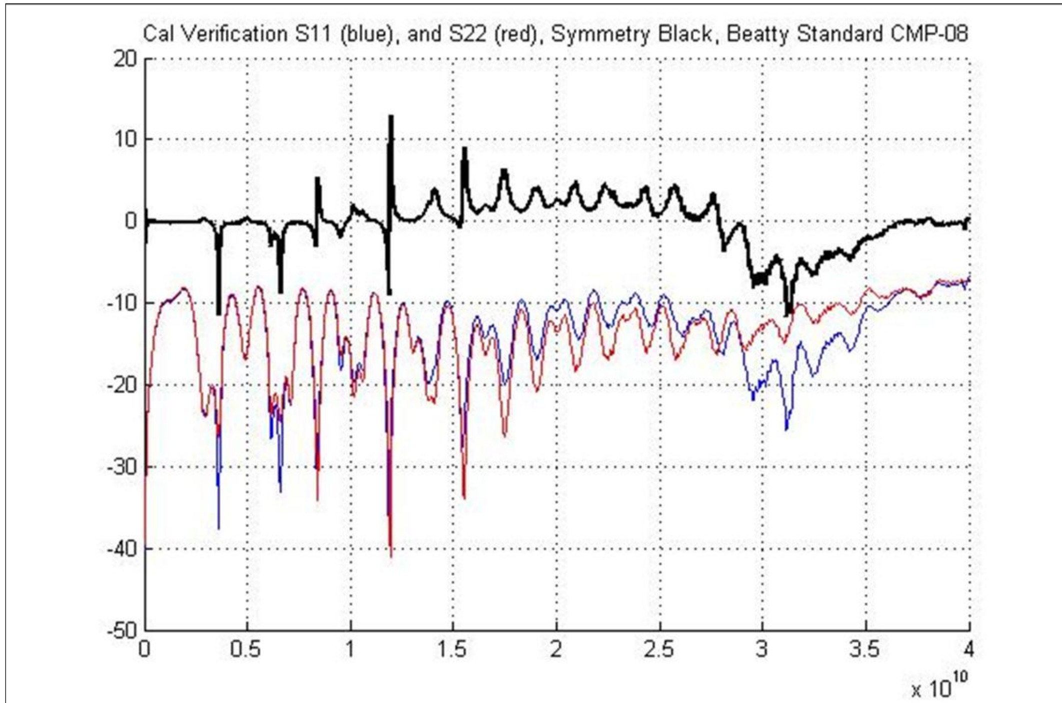

Figure 21 - Calibration verification using 80-Ohm Beatty Standard of Symmetry magnitude error (black line).

Third, for every S-parameter measurement the calibration approach and integrity should be checked [20, 25]. The focus needs to be on the specific measurement objective. We typically check the insertion loss calibration with a KF-KF male-male measurement quality connector (typically this is NOT metrology grade, although it could be a THRU from a suitable calibration kit) and expect <0.1dB of insertion loss variation (dB) and approximately 0.1dB net loss to 40 GHz. This is easily done with a quick linear fit using a MATLAB type tool as shown in Figure 22.

Ports 1 and 2 are Male 2.4mm cable ends, a female KF-KF style connector was used to confirm the calibration of insertion loss (Etf, forward transmission). The connector is not lossless, but the loss is hidden in the variation of 0.1dB of S21 magnitude variation. A simple linear fit of the insertion loss suggests that for these two ports we have a good calibration result and have obtained approximately 0.1dB of insertion loss from the KF-KF connector.

An additional measurement consideration issue is calibration drift. The practice of performing one calibration extending over days or weeks requires validation for every new measurement set. Figure 23 shows an aberration of S21 not evident when calibration was performed. We not only establish the calibration is done satisfaction, but also check the drift if the measurements span more than one 24hour period.

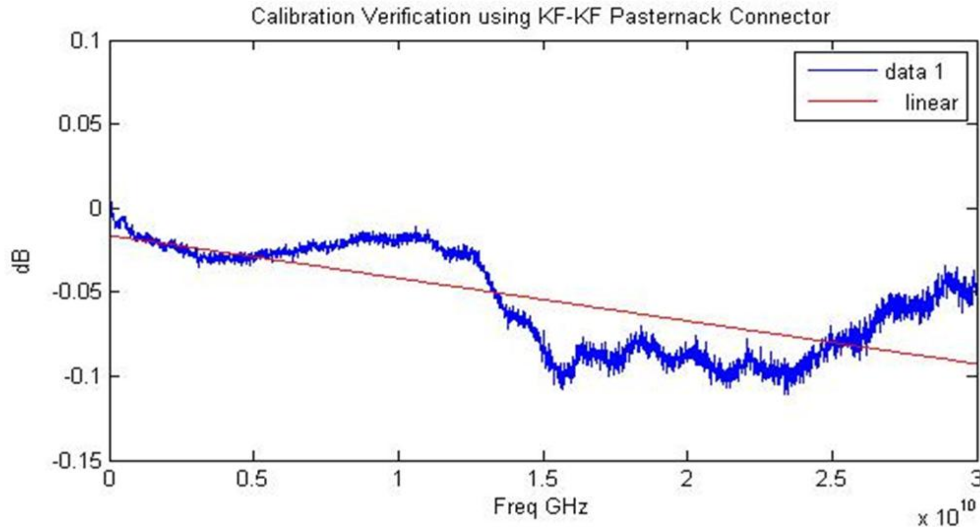

Figure 22 - Example of calibration verification with S21 aberration

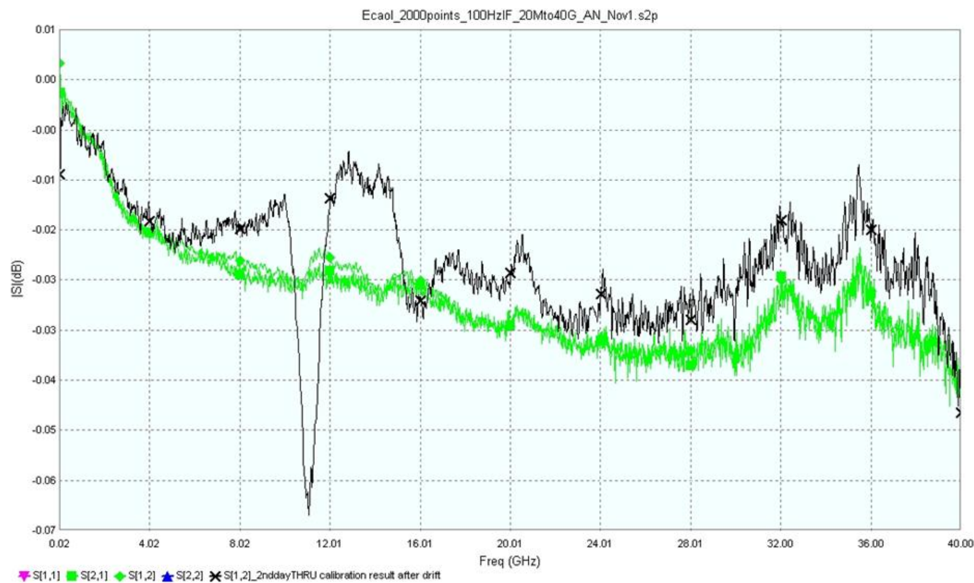

Figure 23 - Example of S21 drift over time

On the day the calibration shown in Figure 23 was performed it appeared to be pristine and did not have any aberrations. This particular VNA showed evidence of excessive drift in a 24 hour period. Although the calibration result in this case may meet our metric of 0.1dB variation over desired frequency span, this aberration reduced confidence in the measurement set up (these types of insertion loss anomalies also create group delay distortion).

Practical Passivity and Causality Verification

A passive device is defined as one that creates no energy into the system, such that the magnitude of each eignenvalue of the S-parameter is less than or equal to one [18, 23]. Some S-parameters may be slightly non-passive due to measurement error (often due to combination of noise, minor calibration residual error and a low-loss device being measured). A common practice is to fix S-parameters by locally adjusting the S-parameter by scaling it with a factor $1/\gamma$,

where γ is the magnitude of the largest matrix eigenvalue. Most measurement related passivity problems are due to calibrations with high residual error, with poor fixture design and de-embedding methods following. General advice is to identify the source of the passivity issue and resolve the problem, **and not locally adjust the S-parameter matrix**. The following example illustrates the methodology of evaluating for passivity.

This procedure is very simple (it does require MATLAB®, RFtoolbox™, this method would also work well with Agilent ADS) SnP Touchstone files of both the measurement and the measurement calibration verification. We first load the SnP file into MATLAB® rfckt.passive object. We simply analyze the result using ispassive.m file included in RFtoolbox™. This generates a matrix and a flag, where the Idx flag indicates whether there was a passivity issue, and the matrix indicates which S-parameters were violating passivity. We then identify the region of the passivity violation more closely.

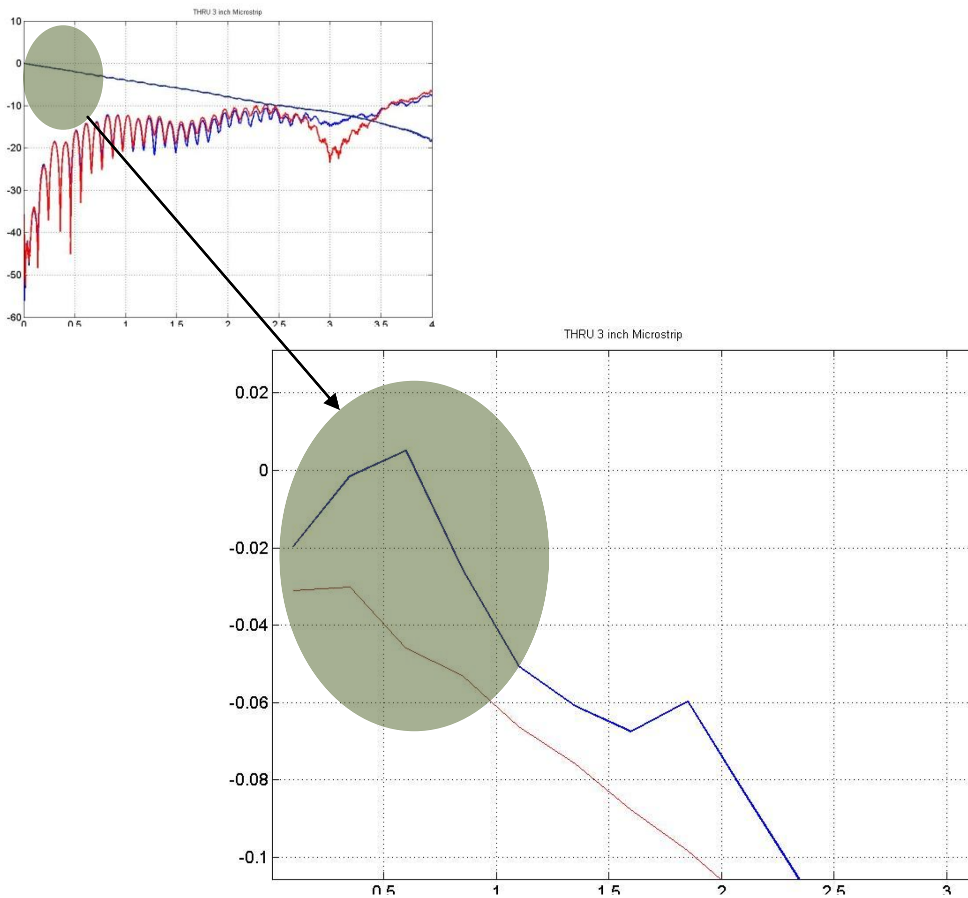

Figure 24 - MATLAB® RFtoolbox™ - measured S-parameter of simple 3 inch THRU showing passivity violation

Measured S-parameter of simple 3 inch THRU indicates there was passivity violation. The problem in S-parameter was isolated by MATLAB® routine to first sampled points at Fstart (around 10-50MHz). Expanding on the magnitude of forward transmission, S21, it is obvious the measurement suggests gain, or passivity violation. It is a common problem to have calibration issues at low frequencies, near the Fstart of the VNA swept measurement.

The passivity problem with 3inch Microstrip THRU measurement is traced back to calibration verification using KF-KF connectors (SOLT calibration was performed at male-male cable ends, so this was not intended for insertable DUT).

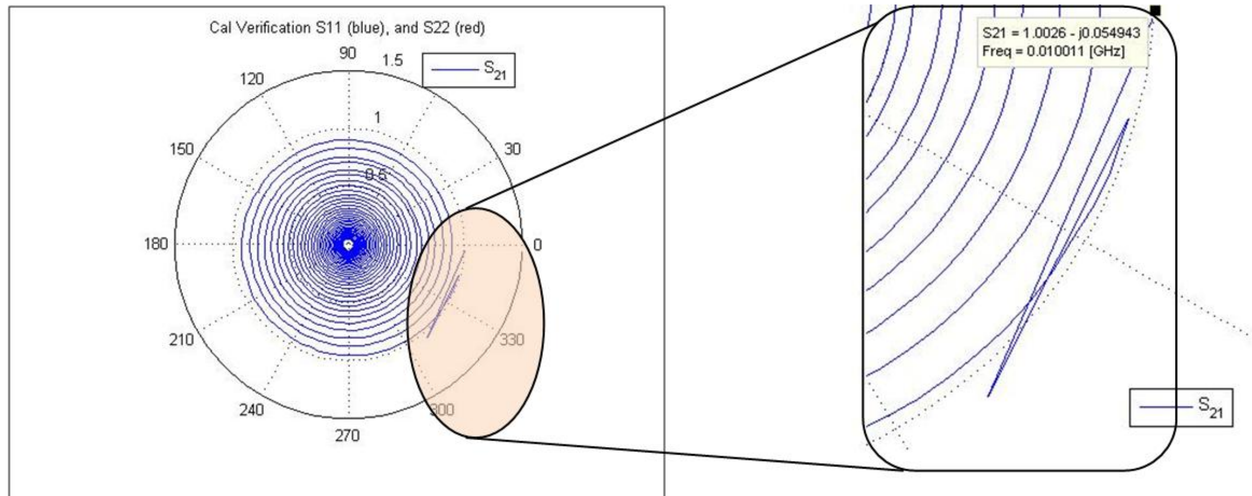

Figure 25 – Expanded region of polar plot of S21 showing evidence of causality violation at lower frequencies

When the S-parameter data is used for 3D EM correspondence minor passivity issues are typically ignored. Another approach is to develop a inherently passive and causal Rational Polynomial fit model of the S-parameter.

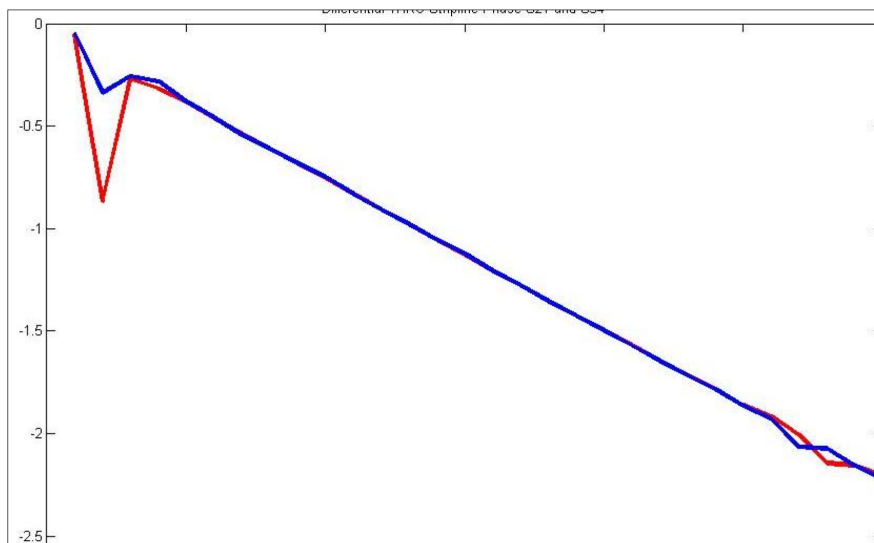

Figure 26 – Validation of KF-KF adapter measurement suggests there are phase and group delay issues at frequencies down near Fstart.

There are numerous practical considerations for making S-parameters that are causal.   Time domain simulation will be distorted and may not converge if S-parameter data is not taken to D.C. Since VNA measurements often typically only go down to 10MHz the D.C. point must be

manually added with simple ohmmeter measurements. Secondly, low frequency region of VNA calibration is a typical hotspot for high residual error for the calibrated VNA.

In addition to providing low frequency D.C. content in the S-parameter, other measurement considerations for causal behavior include making high enough frequency measurements reflecting the signal spectrum. The Fstop frequency is the upper limit of the S-parameter model and needs to cover the bulk of the harmonic energy as seen from resonances and energy in the system. Adequate bandwidth for a given physical system is a really complicated topic. Unfortunately the Kramers-Kronig relationship cannot directly test for causality [16, 17, and 23]. However, we will show a heuristic causality measure using a simple polar plot.

The polar plot method of testing for causality simply checks a polar plot of the S-parameters and verifies that the rotation is clockwise. Examining Figure 23 it is obvious that the rotation for low frequency is not clockwise [19]. Closer examination reveals there were calibration issues at low frequency exhibited by highly non-linear phase of the KFKF adapter measurement. Instead of enforcing causality, we corrected the calibration issue and simply threw out the old measurements.

III. Equalizer Emulation and Virtual Probing

Virtual Probing with Signal Integrity Studio [7]

Step 2 of The Method involves includes the determination of an equalization scheme that can open up a degraded or closed eye. Signal Integrity Studio tool from LeCroy Corporation can be used to simulate the effect a channel or interconnect, showing the output signal and eye along with parametric analysis and jitter decomposition. Users can then apply transmitter and receiver equalization by adding configuring blocks for emphasis (applied to a simulated transmitter signal), Continuous Time Linear Equalization (CTLE), Feed Forward Equalization (FFE) and/or Decision Feedback Equalization (DFE). The output of the equalization stages can then be input to the software's clock recovery algorithm, after which the resulting serial data pattern can be sliced into unit intervals and further analyzed to calculate the resulting eye and jitter values. Figure 27 below shows an analysis of the 11" stripline structure used in this paper. (See labels on the waveforms for descriptions)

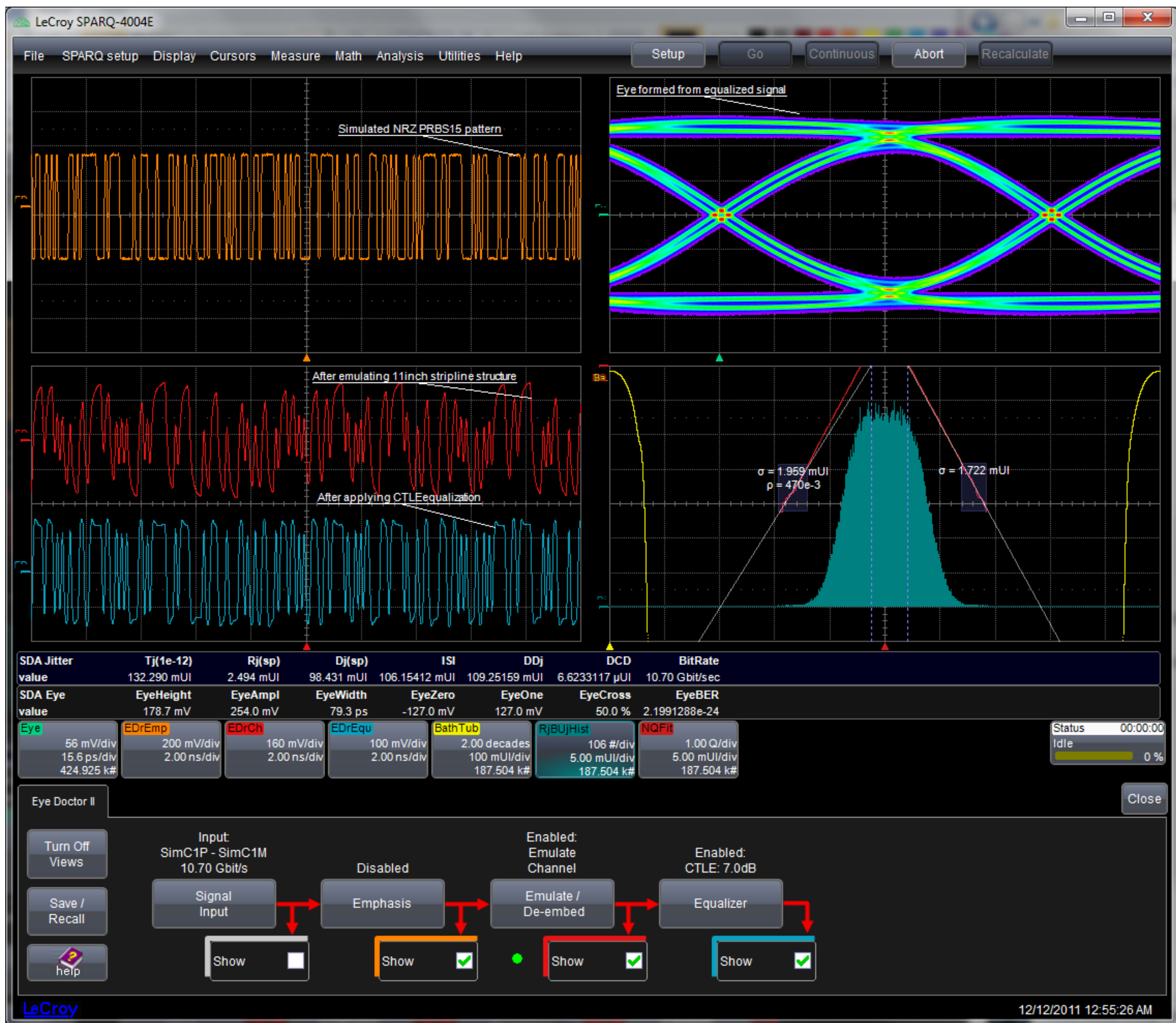

Figure 27 – Screenshot of SI Studio main GUI

Emphasis

Emphasis is added to a signal as a way to pre-compensate for expected channel losses. Since high frequency components are attenuated more by serial data fixtures and channels, boosting the high frequency components (or attenuating low frequency components) can effectively pre-compensate to open up degraded eyes.

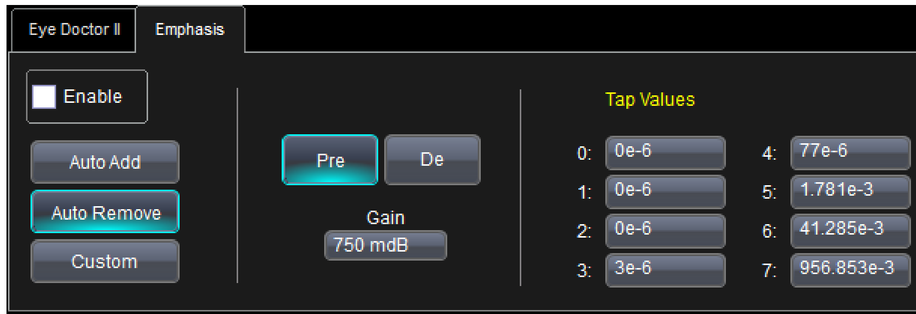

Figure 28 - Screenshot of SI Studio emphasis control settings

Continuous Time Linear Equalization (CTLE)

CTLE is defined by DC gain and the placement of 2 poles and 1 zero. SI Studio includes presets for USB3 and PCIEGen3 standard CTLE equalization schemes (See Figure 29), as well as the ability to set custom values for the poles, zero and gain (See Figure 30). For severely degraded eyes, CTLE can improve the eye to the point where FFE and DFE can be used. (Without CTLE, FFE and DFE training may fail)

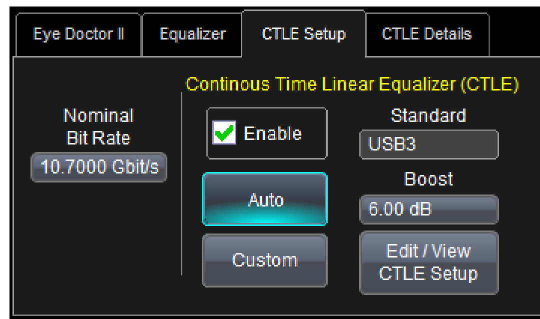

Figure 29 - Screenshot of the SI Studio CTLE control window

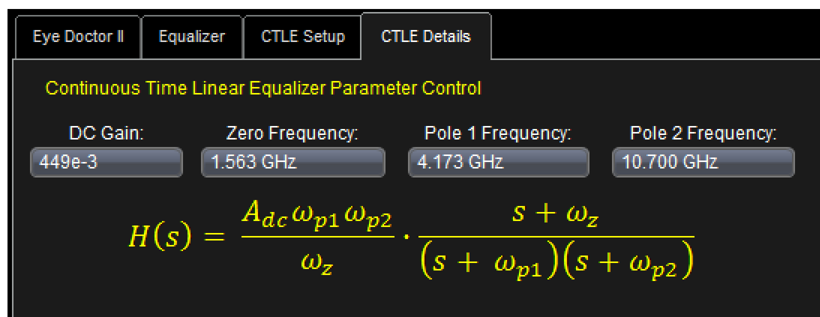

Figure 30 - CTLE parameter control window

Decision Feedback Equalization (DFE)

DFE is a combination of linear and non-linear equalization. DFE takes into account the decoding of bits in the equalization algorithm order to open up the eye.

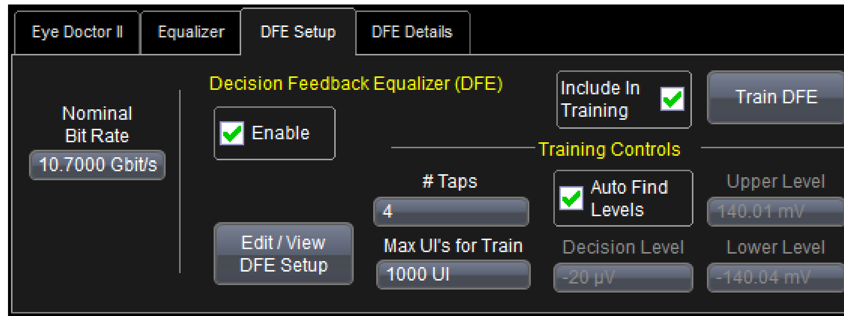

Figure 31 – Screenshot of SI Studio's DFE Control window

Figure 32 - DFE Tap Control window

Feed Forward Equalization (FFE)

FFE is implemented as a 1 tap per unit interval Finite Impulse Response (FIR) filter. This is a linear tapped delay line equalizer. An FFE can compensate for Inter-Symbol Interference (ISI) due to preceding and following bits. Using an FFE introduces a delay in your output waveform. This delay is due to the number of pre-cursor taps.

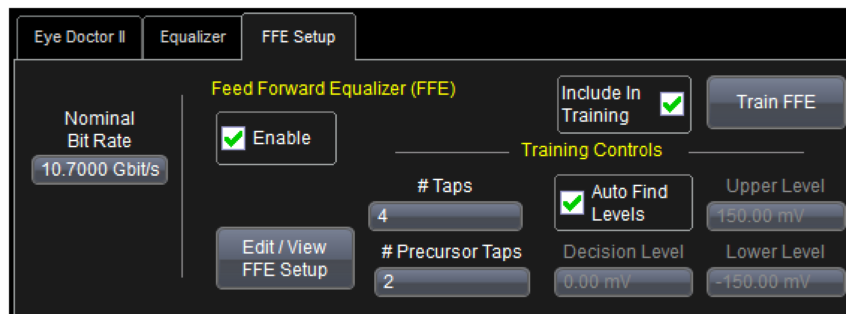

Figure 33 - Screen capture of SI Studio's FFE control window

Figure 34 - FFE Tap window

IV. Receiver Internal Eye Monitoring

In this presentation, we will refer to our internal eye monitor examples as VScope™, the specific implementation patented and used by Vitesse, to avoid confusion with other types of internal waveform monitoring. This architecture has been described at DesignCon 2009[Reference?], so the discussion here will be brief.

VScope™ Architecture [8]

Current generation receive equalizers can easily recover error-free data from what may appear as a completely closed eye when using a conventional oscilloscope to view the waveform. As equalization is embedded into the receiver of an integrated circuit, the output of that equalizer is no longer directly accessible in order to monitor its performance. The system engineer is relegated to probing the input waveform some distance away (outside the chip pins) and trying to extrapolate what the signal might look like at the input to the decision circuit. As input equalizers become more complex and non-linear, the accuracy of extrapolating through them becomes very dubious. The net effect is that receive equalization will effectively obsolete conventional oscilloscopes for signal integrity analysis.

As shown in Figure 35, a probed waveform may not represent actual waveform propagating beyond the probe point. At the input of the semiconductor device where the probe point sits, the oscilloscope shows a degraded waveform. Inside the semiconductor device and beyond the probe point, however, the signal has passed through amplifier & equalization sections in the input section of the chip. So, the signal that the logic portion of the semiconductor receives is significantly different than the probed waveform just outside the semiconductor device.

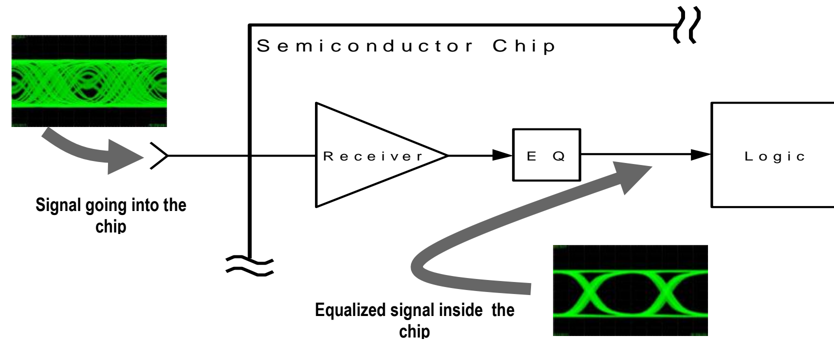

Figure 35: External measurements cannot probe the essential point after the equalizer and before the logic portion of the IC.

A new method to address signal integrity analysis that offers system designers direct access to the signal characteristics within the serial data path without using conventional lab scopes becomes the next logical evolution of test/measurement in signal integrity analysis. Advances in IC designs now offer methods to scan the input data eye within the chip itself and produce a data stream that is representative of the input waveform.

The scanning architecture is based on a dual channel sampling approach (Figure 36) that can be inserted directly in the main data path of the input receiver. The core principle of operation is based on gathering two samples of the input data stream, with each sample point adjustable in voltage and time, with a span that covers both the voltage excursion and bit period of the data signal. The logical result from each sampling channel can be compared on a bit-by-bit basis, and accumulating comparisons over a fixed time period will produce a result similar to a bit-error rate detector. By adjusting the time and voltage offset between the two channels into the error counter, a representation of the input data eye can be created.

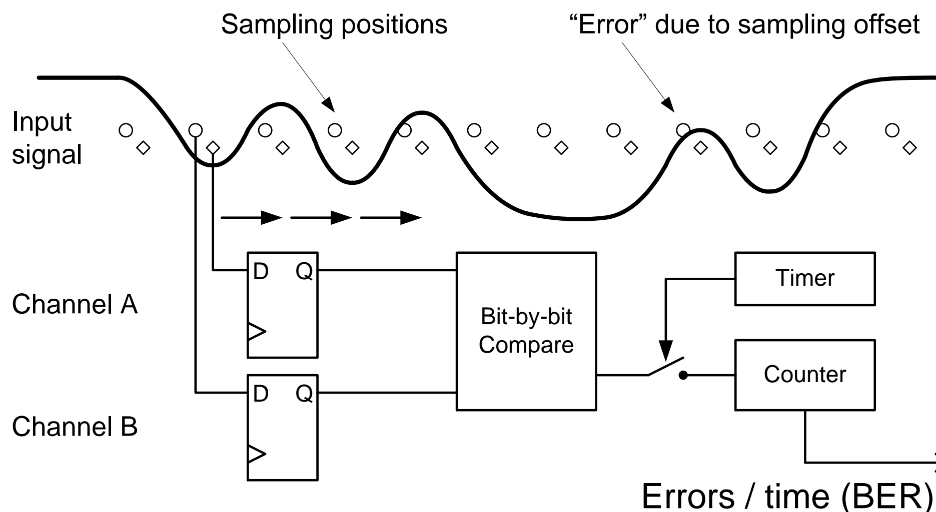

Figure 36: Simplified Embedded Waveform Viewing Architecture

This dual channel approach assures exact correlation between the data gathered and the actual BER performance of the system. This is accomplished by designing both channels to be

identical for tight correlation of system BER. Embedded waveform monitoring technology is also unobtrusive to live data by using one of the channels to carry the live data stream while the other channel, the error channel, scans continuously or on-demand without interfering with the live data. The scanned waveforms are initially processed on chip, and then transported via a separate controller interface to an external CPU for further processing.

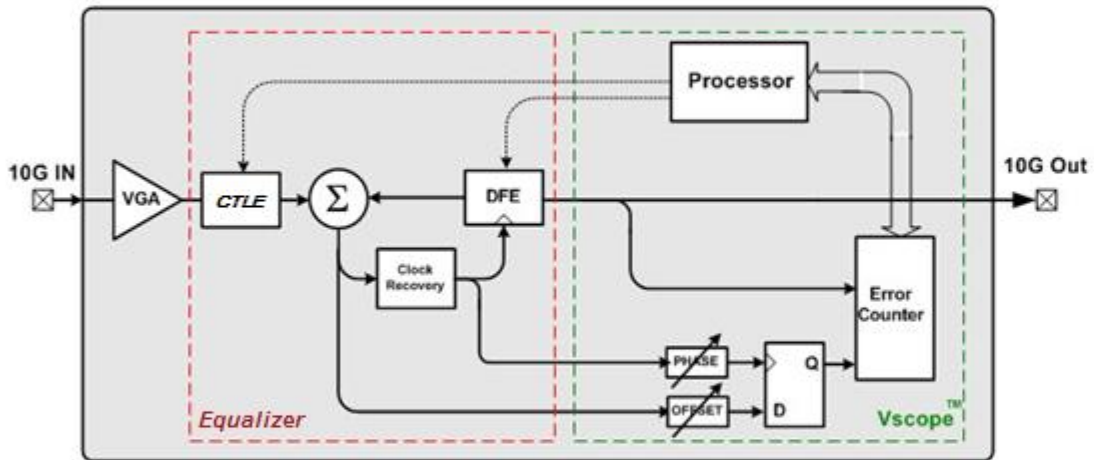

Figure 37: EDC and Embedded Waveform Viewing Architecture

The embedded waveform viewing architecture can be placed into two modes. The in-line diagnostic tool is the first mode, and it allows viewing of the input waveform. This is accomplished by turning off the equalization to become a unity gain amplifier. The link monitor mode is the second mode, and it uses the information on the error channel to optimize the equalizer through an adaptive algorithm for the incoming waveform.

Setup and Data Collection

A 3-tap FIR representing a common transmit architecture was used to drive the test channels. A common receive architecture including a high dynamic range CTLE implementation and a 4-tap DFE structure was used for all channels under test.

Embedded Waveform Viewing on-chip image fidelity is illustrated using the same three Stripline lengths on the Wild River Technology® CMP platform used in section 3 with the SI Tool. For each channel length examined, the line rate and data pattern were 10.70 Gbps and PRBS 2^15-1 respectively. Transmit settings were fixed for all tests with the following setting: C-1=-.75 mA, Co=12.0 mA, C+1 = -1.25 mA.

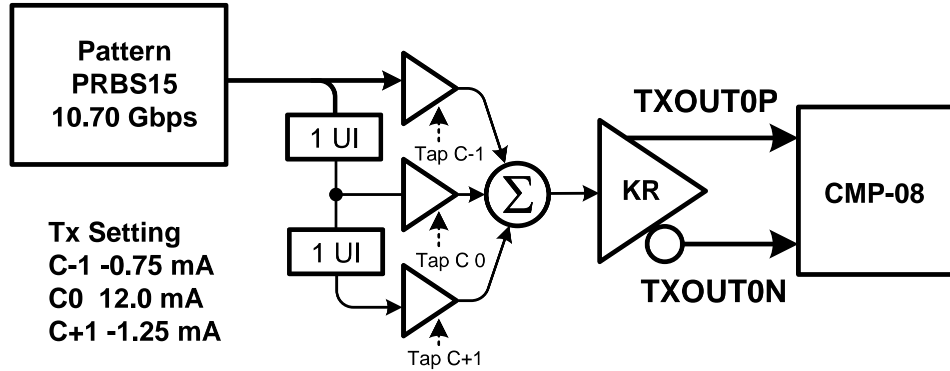

Figure 38: Transmitter Pre, Main and Post-Cursor settings

Using the same Wild River Technology® test platform a fourth test case was also examined that included several coupled structures intended to simplify cross talk injection and testing. The fourth case will be discussed in Section 5.

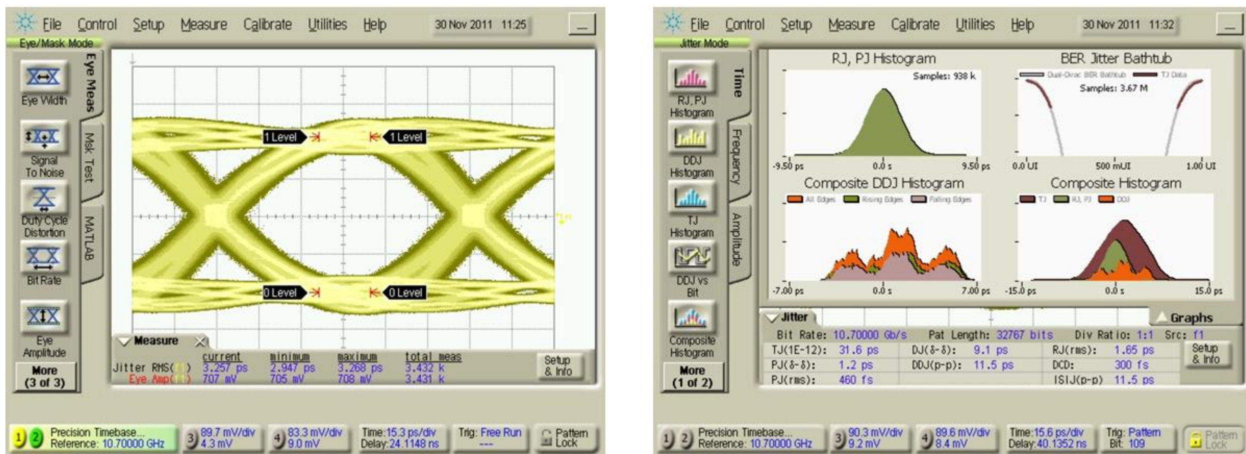

Figure 39: Transmit Output Eye and Jitter

VScope™, Data and SI Tool Correlation

Waveforms captured by the eye monitor enabled IC circuits show sufficient correlation with the bench top instrument, in this case the J-BERT, to develop eye metrics capable of driving receiver equalization settings to near optimum positions for CTLE and DFE enabled receiver architectures. The following table shows, for each of the 1st three test cases (without NEXT), the Signal Integrity Studio tool eye diagram and the Vitesse embedded waveform eye diagram. From the high fidelity embedded waveform data, several eye metrics can be developed that provide valuable signal integrity information useful for maintaining optimal link margins.

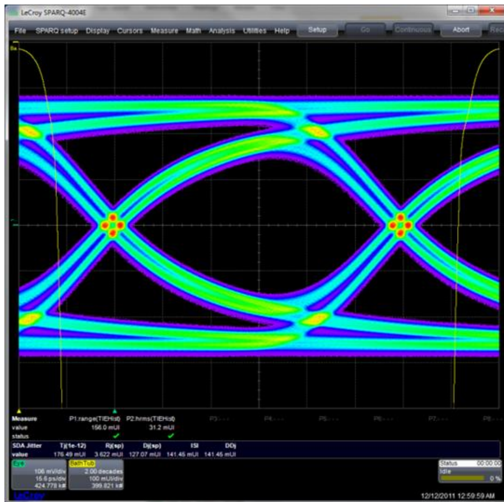
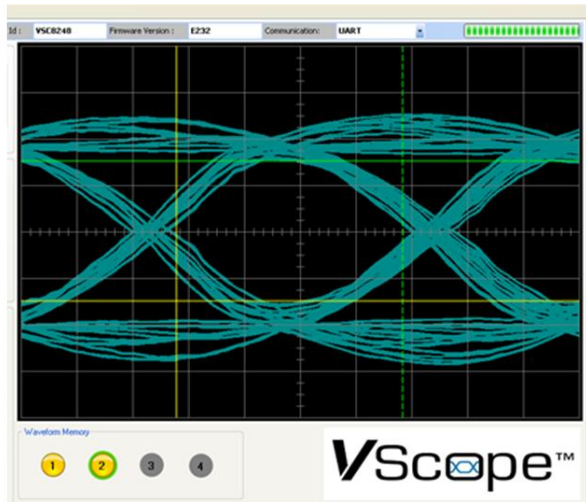

Figure 40: Case 1 - 3 inch Strip-Line Diff Pair no EQ (Studio Simulation vs. VScope)

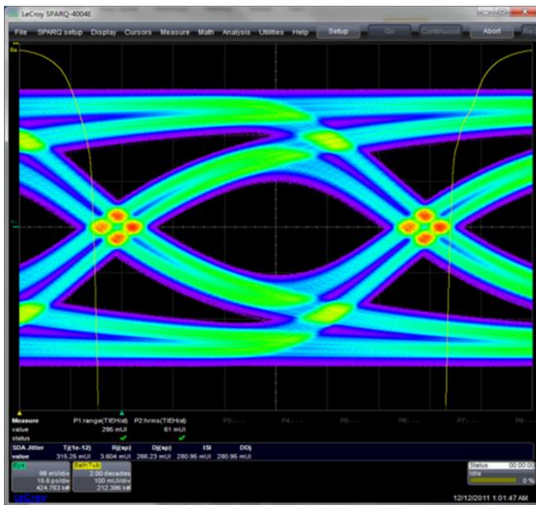
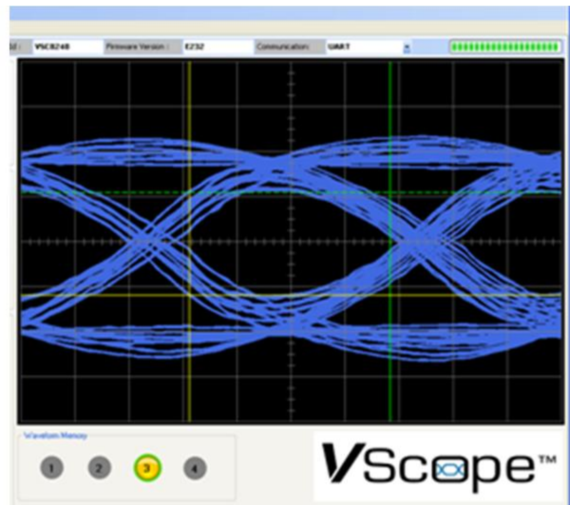

Figure 41: Case 2 - 6 inch Strip-Line Diff Pair no EQ (Studio Simulation vs. VScope)

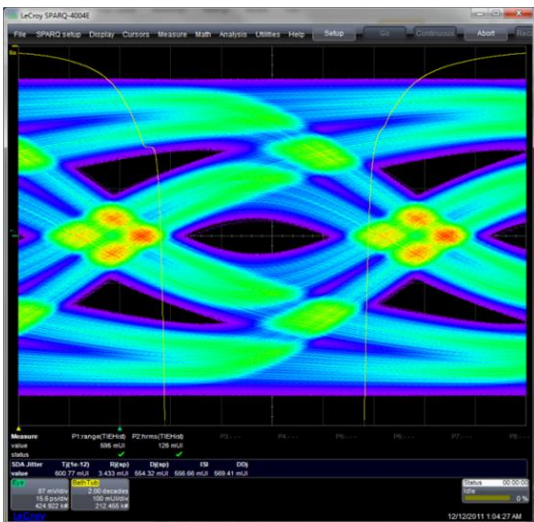
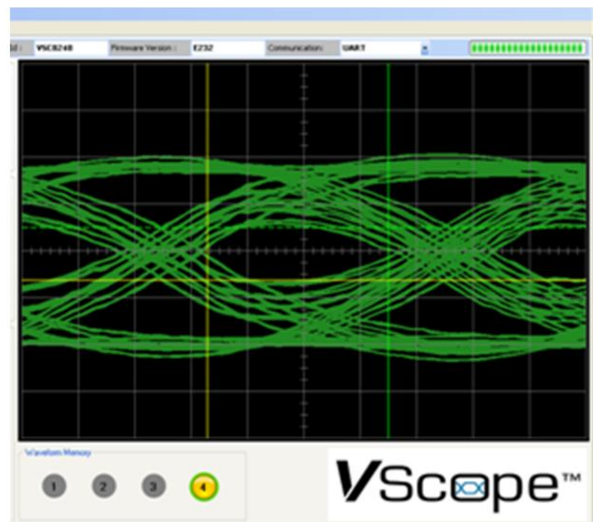

Figure 42: Case 3 - 11 inch Strip-Line Diff Pair no EQ (Studio Simulation vs. VScope)

V. Equalization Optimization with Crosstalk Aggressed Channels

Equalizer Optimization in the High Crosstalk Environment

As technology advances to higher data rate systems, isolation of signals between neighboring channels becomes more difficult. While losses increase with frequency, isolation decreases with frequency. Poor isolation introduces crosstalk as bounded uncorrelated jitter to our signal.
For most standards at 10GbE, the reference receiver and transmitter are based on 3 types of equalization architecture: Continuous Time Linear Equalizer (CTLE), Feed Forward Equalizer (FFE), and the Decision Feedback Equalizer (DFE). All 3 are capable of shaping the frequency – loss curve to compensate or reverse the channel effects. Each has their strengths and weaknesses to attack specific problems.

When it comes to cross-talk environments, the FFE and CTLE either maintain or increase the Signal to Noise ratio (SNR). These 2 equalization architectures will amplify higher frequencies relative to lower frequencies to compensate for channel losses as expected. While amplifying the higher frequency signal is good to compensate for losses, it will also amplify the high frequency crosstalk bleeding over from neighboring channels. Because isolation decreases with frequency, most of the crosstalk is in the higher frequencies. Therefore, the FFE and CTLE architectures enhance the noise in the system.

In contrast, the DFE architecture applies corrections after a bit decision has been made and does not add noise. This equalizer leverages its decisions back to the input of its equalization filter. By doing so, the incoming signal is re-enforced w/ “clean” decisions that effectively increases the Signal to Noise ratio (SNR). Depending on the channel and noise characteristics, the DFE will provide at least 2 dB of output SNR improvement over CTLE and FFE equalizers [9].
In practice, a high crosstalk system benefits by applying more DFE over CTLE or FFE equalization. One trade-off to keep in mind is the error propagation of the DFE (although FEC coding could mitigate this effect). Therefore, it’s best to characterize a system and understand its SNR requirements and trade-off the amount of DFE vs. CTLE/FFE needed.

Case4: VScope™ as a Signal Integrity Tool

In our case 4, we use a new 11 inch broadside coupled channel (illustrated in Figure 43) in order to introduce crosstalk in varying degrees: Minimum, Medium, and Maximum.

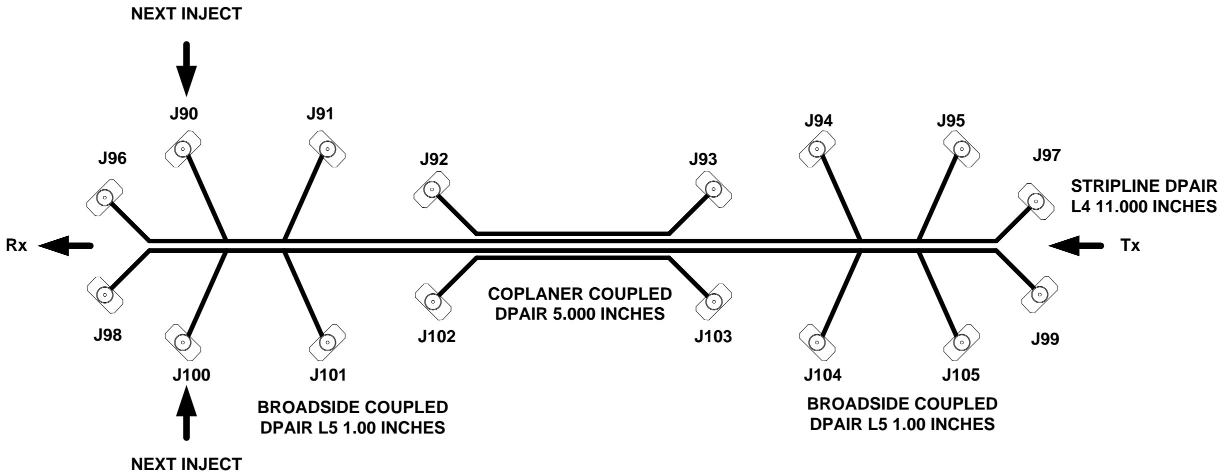

Figure 43: Case4: 11 inch Strip-line differential pair with two 1 inch broadside coupled differential pairs and one 5 inch co-planar coupled differential pair

Internal IC waveform eyes are superimposed in Figure 44 below showing the effects of 3 levels of NEXT and NEXT squelched.

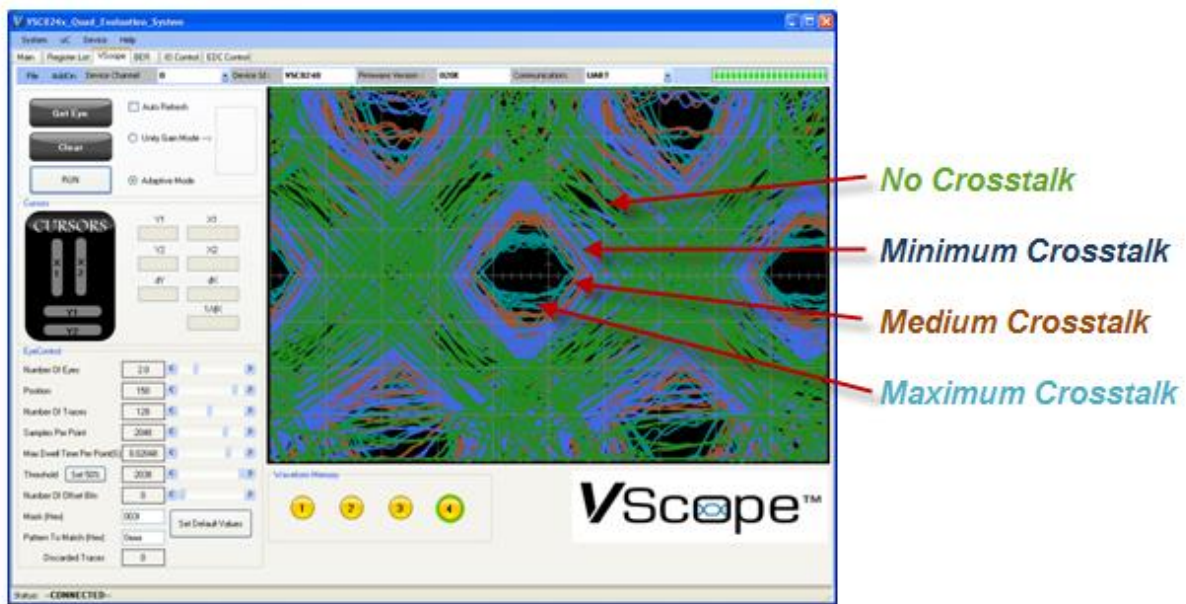

Figure 44: Crosstalk eyes overlaid

The VScope™ Eye metric used is the best phase, and the max inner vertical opening at that phase. One of the metrics developed from the internal eye telemetry and used to drive the equalization engine is called "Eyescore" and is shown in Table 1 for the 4 levels of NEXT applied in case 4. Eyescore is inversely proportional to inner eye opening.

NEXT Level	EyeScore (Converted to Decimal)
Off	192k
Minimum	314k
Medium	377k
Maximum	476k

Table 1 - NEXT levels vs. VScopeTM "Eyescore"

The Equalizer is further adjusted based upon Eyescore values which are shown to correctly respond to increasing levels of NEXT interference. To show the effect of the NEXT levels on the receiver post equalization, BER-V curves predict that we have better than a 1.0x E-14 system without crosstalk and for the MIN-NEXT and MED-NEXT levels of cross talk. For the MAX_NEXT case we record 3.4E-13 – very close to what is estimated in Figure.

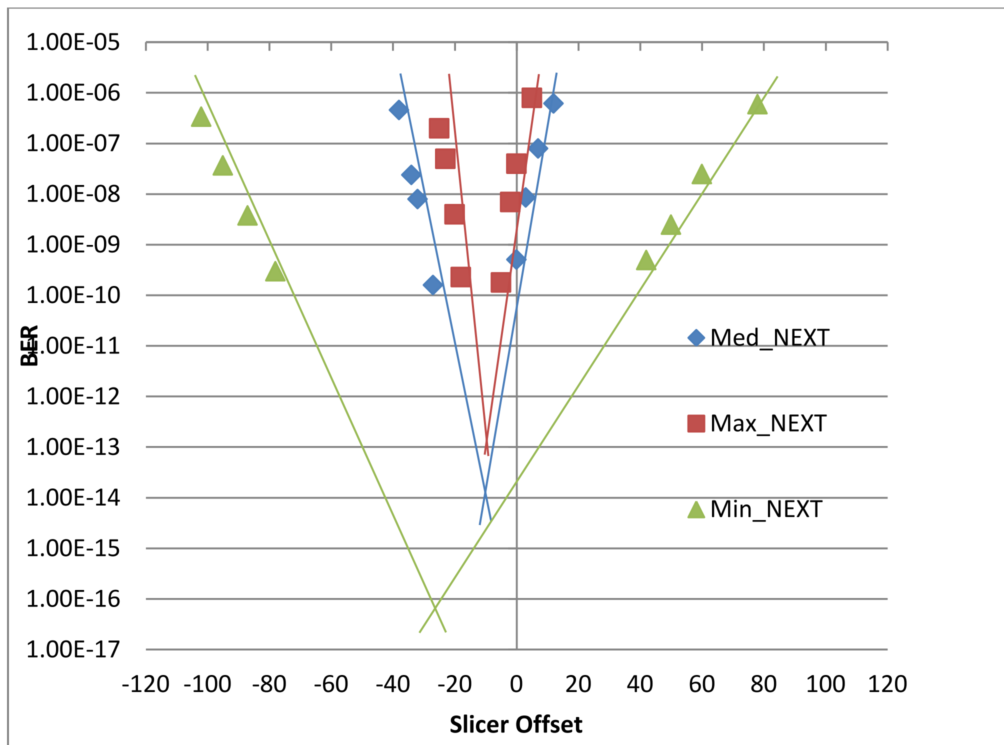

Figure 45: Case 4: 11 Inch Strip-Line Differential Pair BER-V curves for three levels of NEXT

At the receiver, after equalization optimization, the slicer offset is adjusted away from optimum and the BER recorded for multiple settings to develop the BER-V curves shown in Figure 45. There is shown to be good correlation between measured BER and the predicted BER from these curves. The on-chip ability to predict expected BER combined with the on-chip embedded waveform viewer are powerful tools for the signal integrity Engineer.

Receiver Performance Improvement

With the aid of the internal eye metrics, additional Case 4 test data was developed that showed an important relationship between the equalization effectiveness of the CTLE strength and the DFE contribution for the different levels of crosstalk.

To achieve the BER-V performance shown previously in the presence of severe NEXT required a significant increase in the DFE contribution while minimizing the CTLE setting. Figure 46 illustrates this finding. The additional DFE contribution is shown to improve the receiver equalization performance in high crosstalk environments.

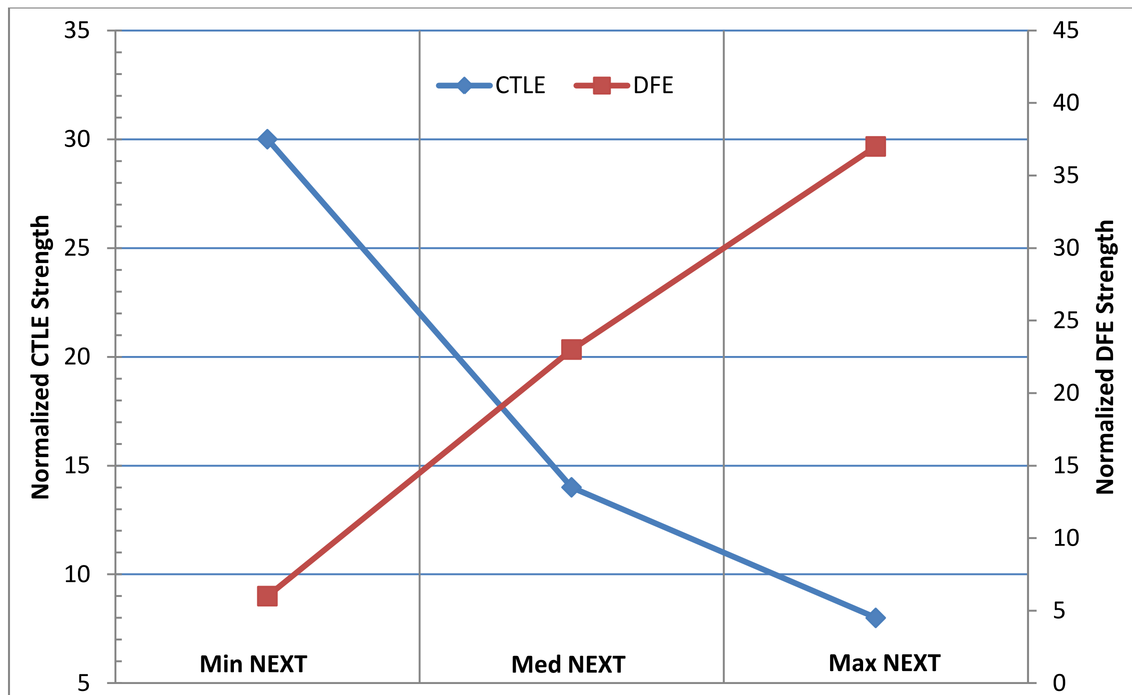

Figure 46: Case 4 CTLE and DFE trading off equalization strength in the face of varying amounts of crosstalk

Table 2 shows the voltage margin in the BER-V curve by comparing the 3 sets of CTLE and DFE equalization settings in the maximum NEXT level environment. Trading off the CTLE for more DFE equalization shows that the voltage margin improves from no margin.

NEXT Level	CTLE (EQ Strength)	DFE (EQ Strength)	Voltage Margin @ 1e-12 BER (mV)
Maximum	30	6	0
Maximum	14	22	0
Maximum	8	37	5

Table 2: BER-V Margin Improvement with more DFE

VScope^{TM} or internal eye monitoring is a powerful tool for the signal integrity Engineer when used as an aid to develop link margin metrics that are not possible to get otherwise.

Emphasizing the levels of DFE equalization when there is significant crosstalk present can yield better link margin over pure CTLE based equalization based only on the IL characteristics of the link.

VI. Conclusions and Summary – and Future Direction

By integrating a library of tested S-parameter data-mined libraries along with a perfect TX/RX emulation tool, and then monitoring the eye integrity with internal silicon we have demonstrated a complete and robust method for the problem of closed eyes due to severe channel pathology.

Future direction suggests closer examine of high levels of modality, different contributions of RJ versus BUJ types of crosstalk jitter and examining the impact of DCD.   It would also be a good direction to formalize this method as a means of improving RX jitter tolerance in actual systems.

Bibliography

[1] Y. Shlepnev, A. Neves, T. Dagostino, S. McMorrow, "Practical identification of dispersive dielectric models with generalized modal S-parameters for analysis of interconnects in 6-100 Gb/s applications", Proc. of DesignCon 2010.

[2] J. Bell, S. McMorrow, M. Miller, A. Neves, Y. Shlepnev, Developing Unified Methods of 3D Electromagnetic Extraction, System Level Channel Modeling, and Robust Jitter Decomposition in Crosstalk Stressed 10Gbpsec Serial Data Systems, Proc. of DesignCon 2011

[3] D. Dunham, J. Lee, S. McMorrow, Y. Shlepnev, Design and Optimization of a Novel 2.4 mm Coaxial Field Replaceable Connector Suitable for 25 Gbps System and Material Characterization up to 50 GHz, Proc. of DesignCon 2011

[4] Y. Shlepnev, C. Nwachukwu, Roughness characterization for interconnect analysis, Proc. of the 2011 IEEE International Symposium on Electromagnetic Compatibility, Long Beach, CA, USA, August, 2011, p. 518-523.

[5] Y. Shlepnev, S. McMorrow, "Nickel characterization for interconnect analysis", Proc. of the 2011 IEEE International Symposium on Electromagnetic Compatibility, Long Beach, CA, USA, August, 2011, p. 524-529.

[6] Simbeor Electromagnetic Signal Integrity Software, www.simberian.com

[7] P. Pupalaikis, Advanced Tools for High Speed Serial Data Measurements: Equalizer Emulatin and Virtual Probing, Proc. Of DesignCon 2007

[8] G. Noh, T. Coe, A. Balcioglu. "Utilizing Electronic Dispersion Compensation (EDC) and Embedded Waveform Viewing Technologies in Next Generation Backplanes", 13-TH1 DesignCon 2009.

[9] Thomas Starr et al, "DSL Advances", Prentice Hall Professional, January 2003, page 120

[10] James F. Buckwalter, Analysis and Equalization of Data-Dependant Jitter, ISCC, March 2006

[11] Michael Steinberger, SiSoft Corp., Comparison of BER Estimation Methods which Account for Crosstalk, Proc. of DesignCon 2009

[12] J. D'Ambrosia, A. Healey, Backplane Channels and Correlation Between Their Frequency and Time Domain Performance, Proc. of Euro DesignCon 2005

[13] Mike Li, M. Shimanouchi, S. Narayan, W. Wong, S. Shumarayev, Architecture and Configuration Explorations for 28 Gbps I/O Links, Proc. of DesignCon 2011

[14] Chris Loberg, Serial-Data Link Testing in the "Eye", Electronic Design, 9/10

[15] V. Stajonanovic, M. Horowitz, Modeling and Analysis of High-Speed Links, Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003, Sep 2003

[16] C. Warwick, White Paper: Understanding the Kramers-Kronig Relation Using a Pictorial Proof, Agilent Technologies, Mar 2010

[17] C. Warwick, F. Rao, App note: S-parameters Without Tears, Agilent Technologies, Jan 2010

[18] P. Triverio, Stability, Causality, and Passivity in Electrical Interconnect Models, IEEE Transactions on Advanced Packaging, Nov 2007

[19] Y. Shlepnev, Quality of S-Parameter Models, www.simberian.inc

[20] R. Schaefer, Agilent Corp., Comparison of Fixture Removal Techniques for Connector and Cable Measurements

[21] Heidi Barnes, Verigy, The Art of VNA Calibrations for Measuring Low Loss PCB Components, IEEE MTT International Microwave Symposium, May 2010

[22] Cadence Corp., App note: Guidelines for Robust S-Parameter Model Development, Cadence Design Systems, Inc., June 2004

[23] C. Morgan, Solutions for Causal Modeling and A Technique for Measuring Causal, Broadband Dielectric Properties, Proc. of DesignCon 2008

[24] A. Neves, Webinar: Calibration and De-Embedding Techniques In the Frequency Domain, www.WildriverTech.com