DesignCon 2012

WHERE CHIPHEADS CONNECT

Robust Method for Addressing 12 Gbps Interoperability for High-Loss and Crosstalk-Aggressed Channels

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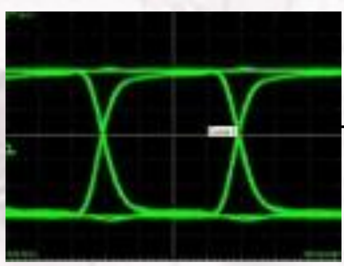
- Conundrum
  - a: a question or problem having only a conjectural answer
  - b: an intricate and difficult problem

- Conjectural
  - a: interpretation of omens
  - b: a conclusion deduced by surmise or guesswork

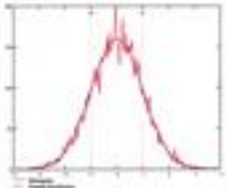
So, you probably asking “where is he going with these definitions?

Practical Channels Close Down Eyes for High Data Rates

TX

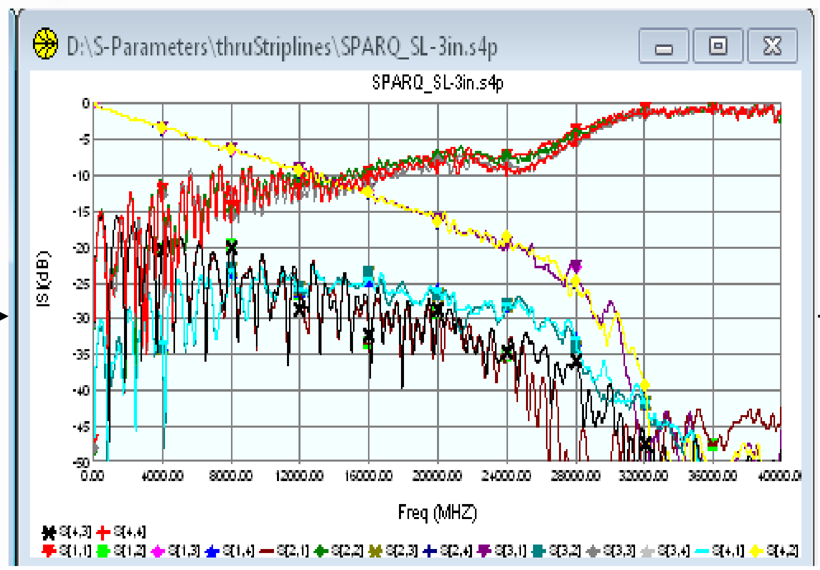


n_x



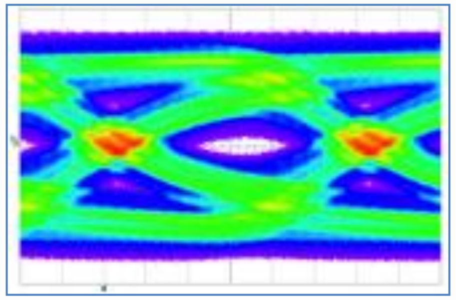
Gaussian Noise

S-Parameter Model of Channel



- **Insertion Loss**
- **Return Loss**
- **Impedance Variations**
- **Resonance**
- **Crosstalk**

RX



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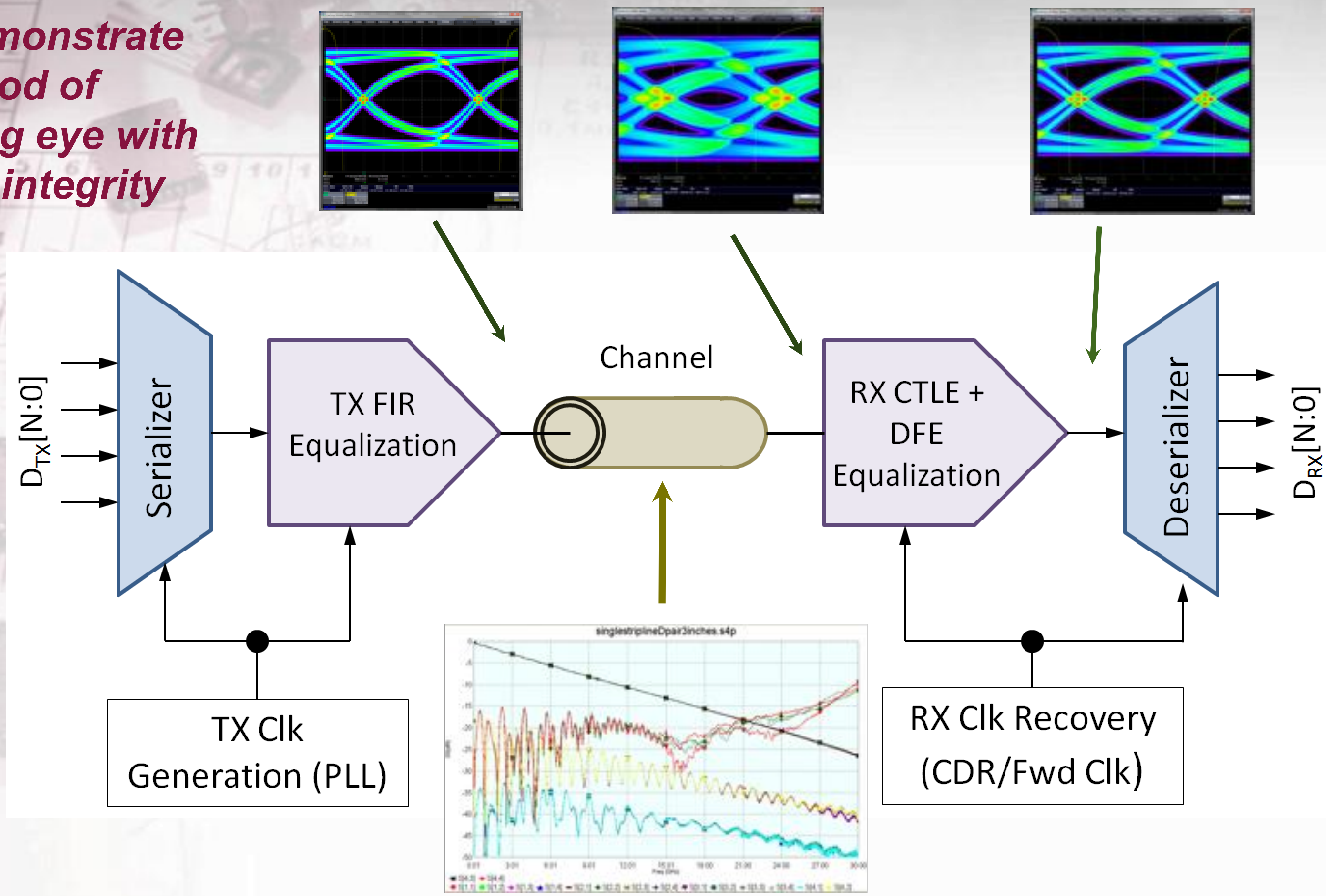
The Problem or Conundrum Becomes:

1. How do I open the eye?
2. What do I attack first?
3. How do I confirm my suspicions?
4. How do I optimize for both Loss and Crosstalk aggression
5. How do I develop a concerted method to make my job easier!

We demonstrate a method of opening eye with higher integrity



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The Method:

1. Start with a Family of S-Parameter Models.
2. Test the S-parameters
   - Tested for Passivity/Causality
   - Measurement Validated
3. Data-Mine the S-parameter in library

Sources of S-parameter Library

Integrated Channel Model Platforms

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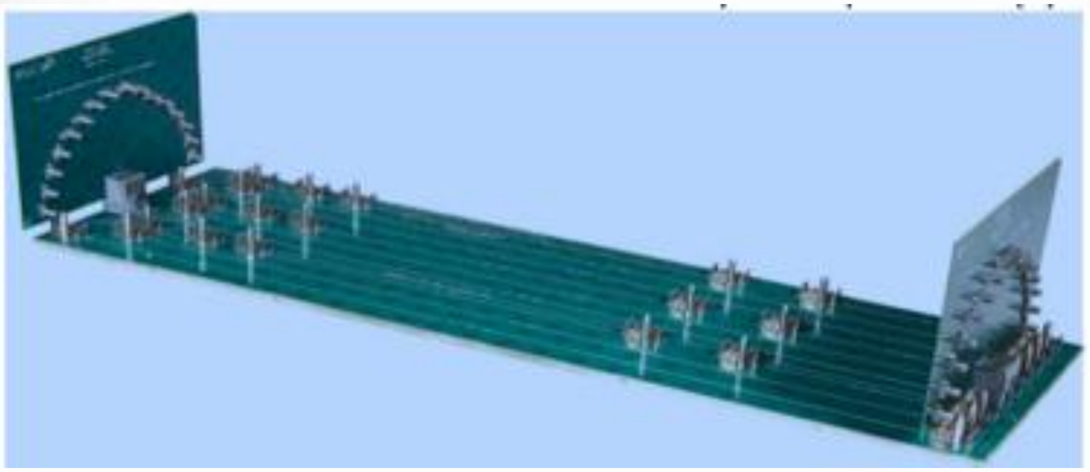
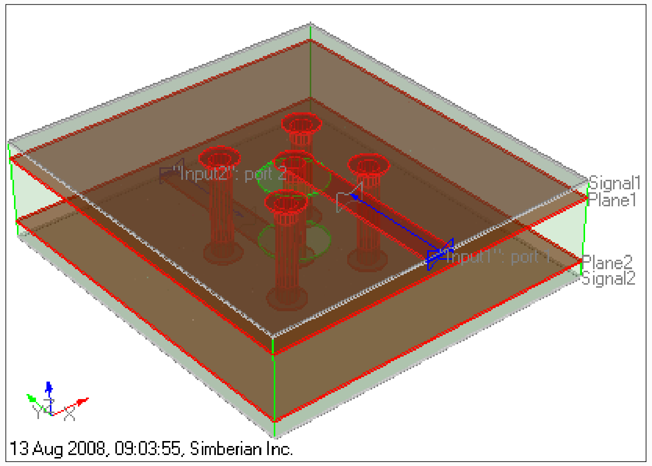


Backplane - Application Specific

VITESSE



3D EM

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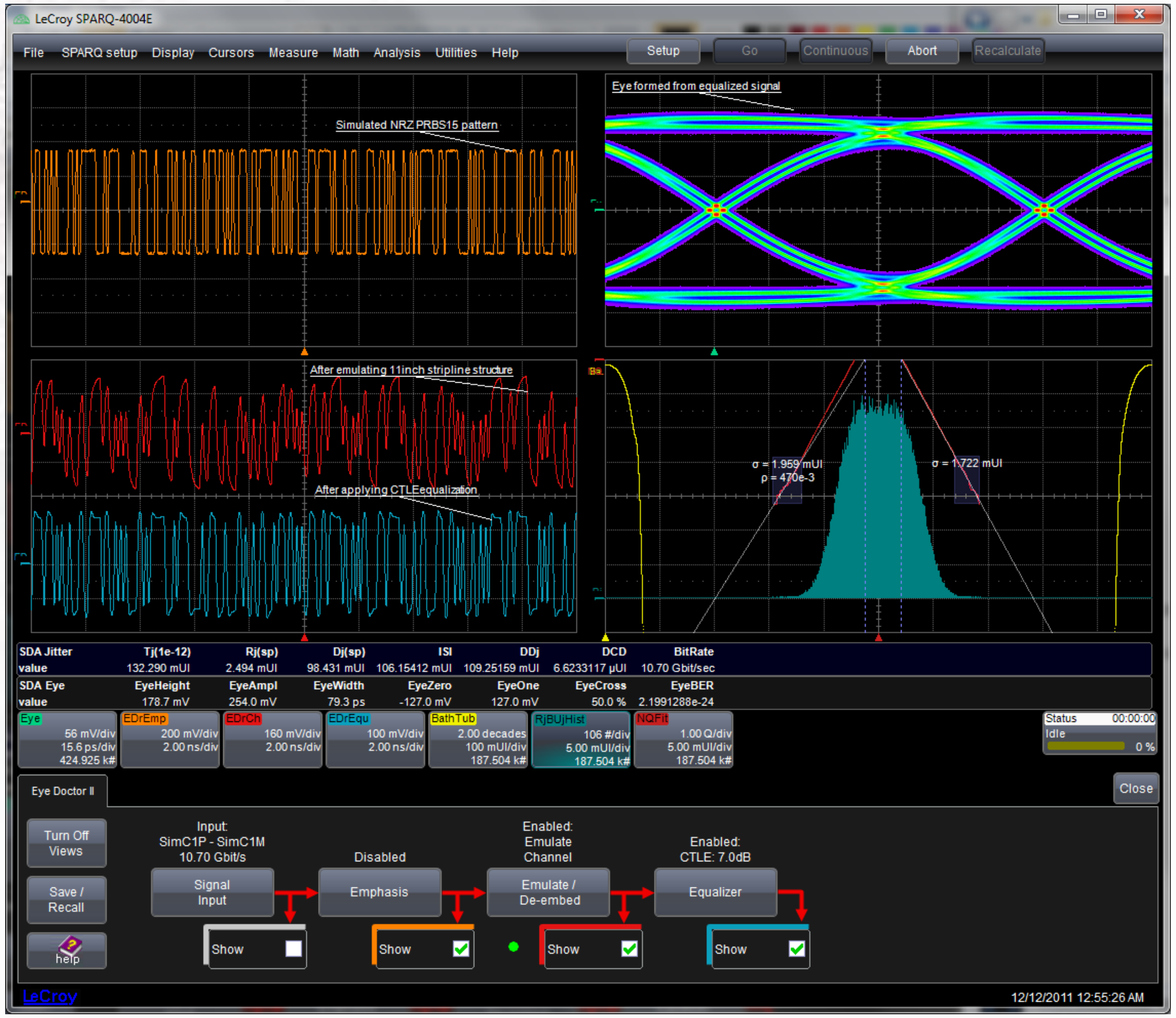
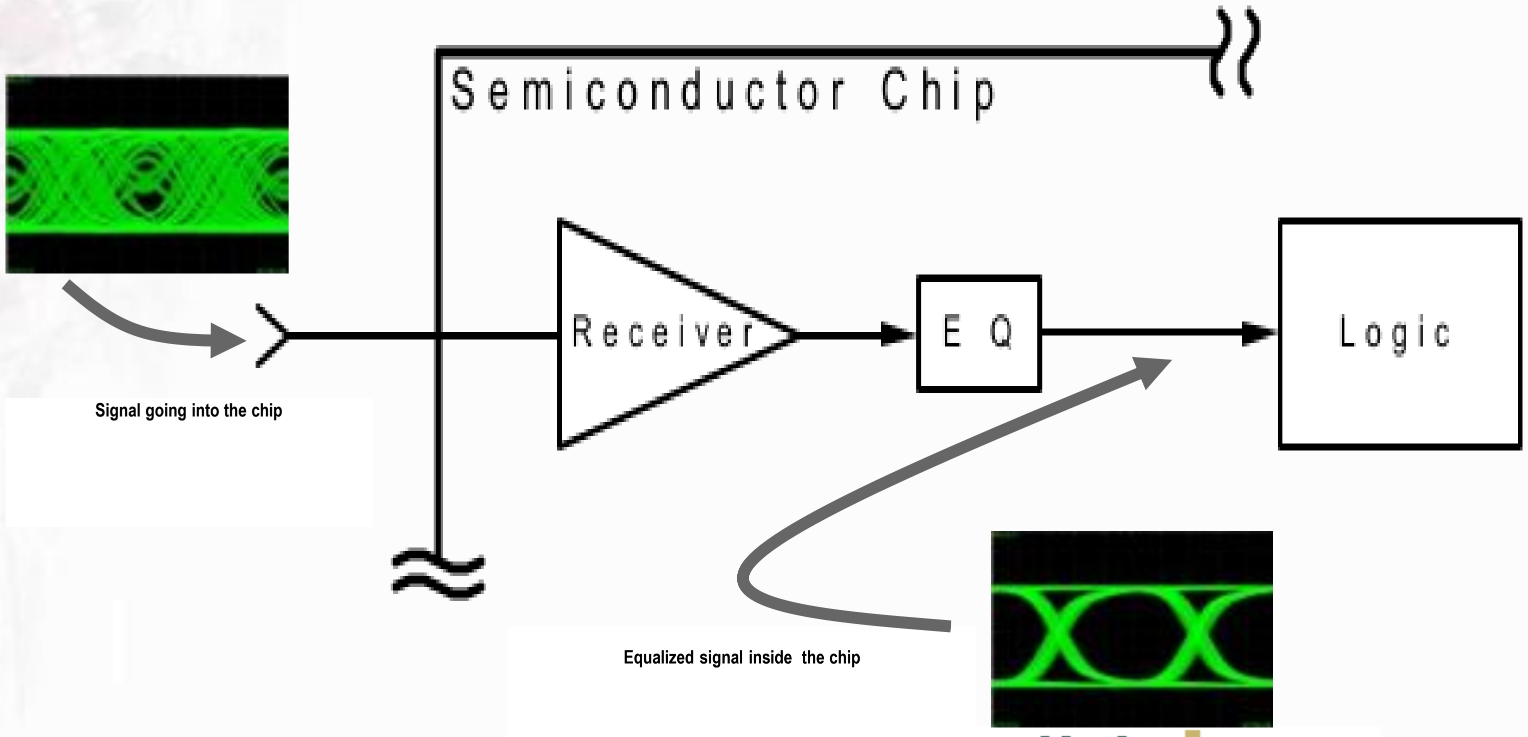
4. Emulate Silicon SERDES architecture with EDA tool. We create a perfect TX/RX.



5. After EDA tool optimization establishes optimal eye opening, implement physical silicon+Channel, monitor eye internally
6. Correspond to EDA tool optimized result
7. Optionally add crosstalk aggression and re-optimize.



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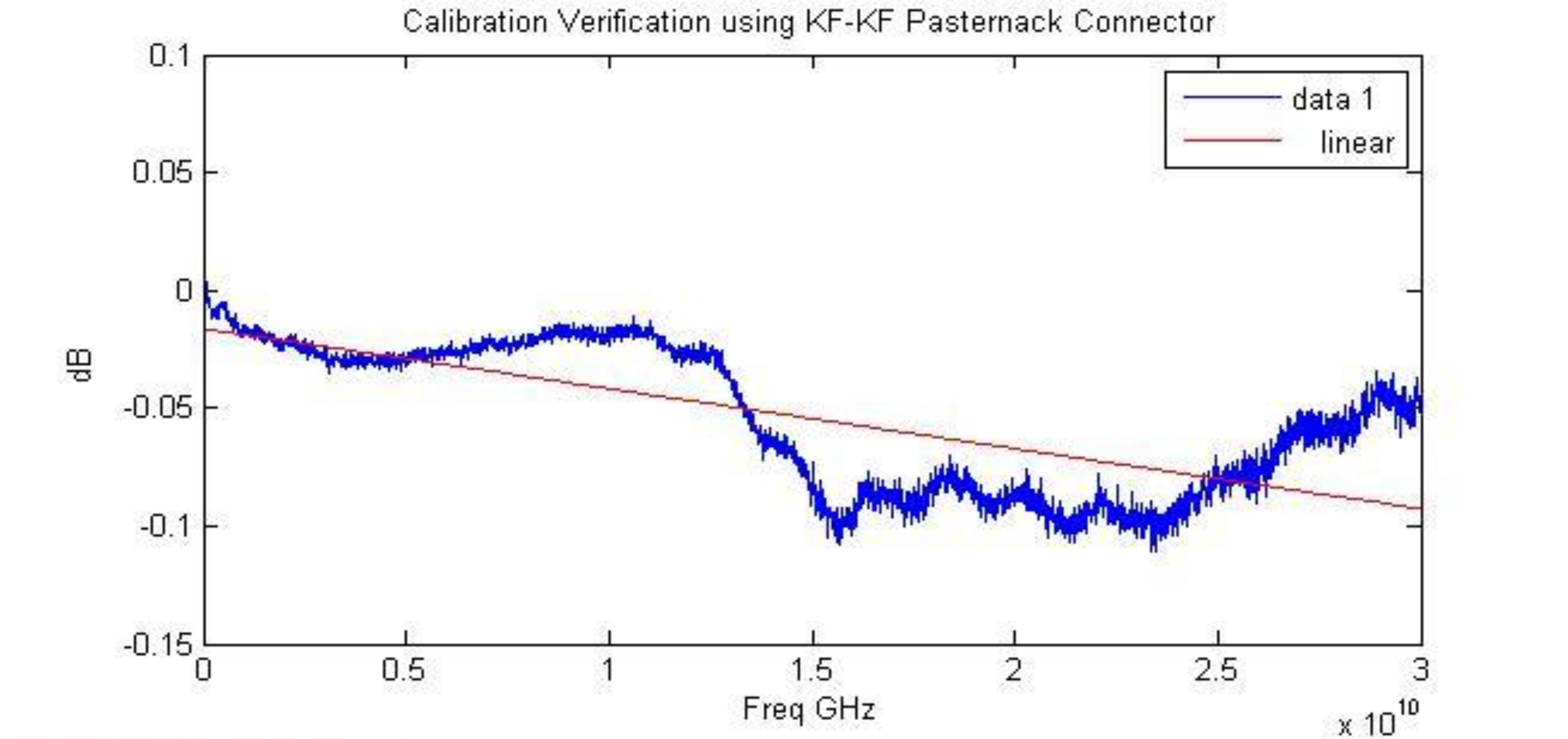
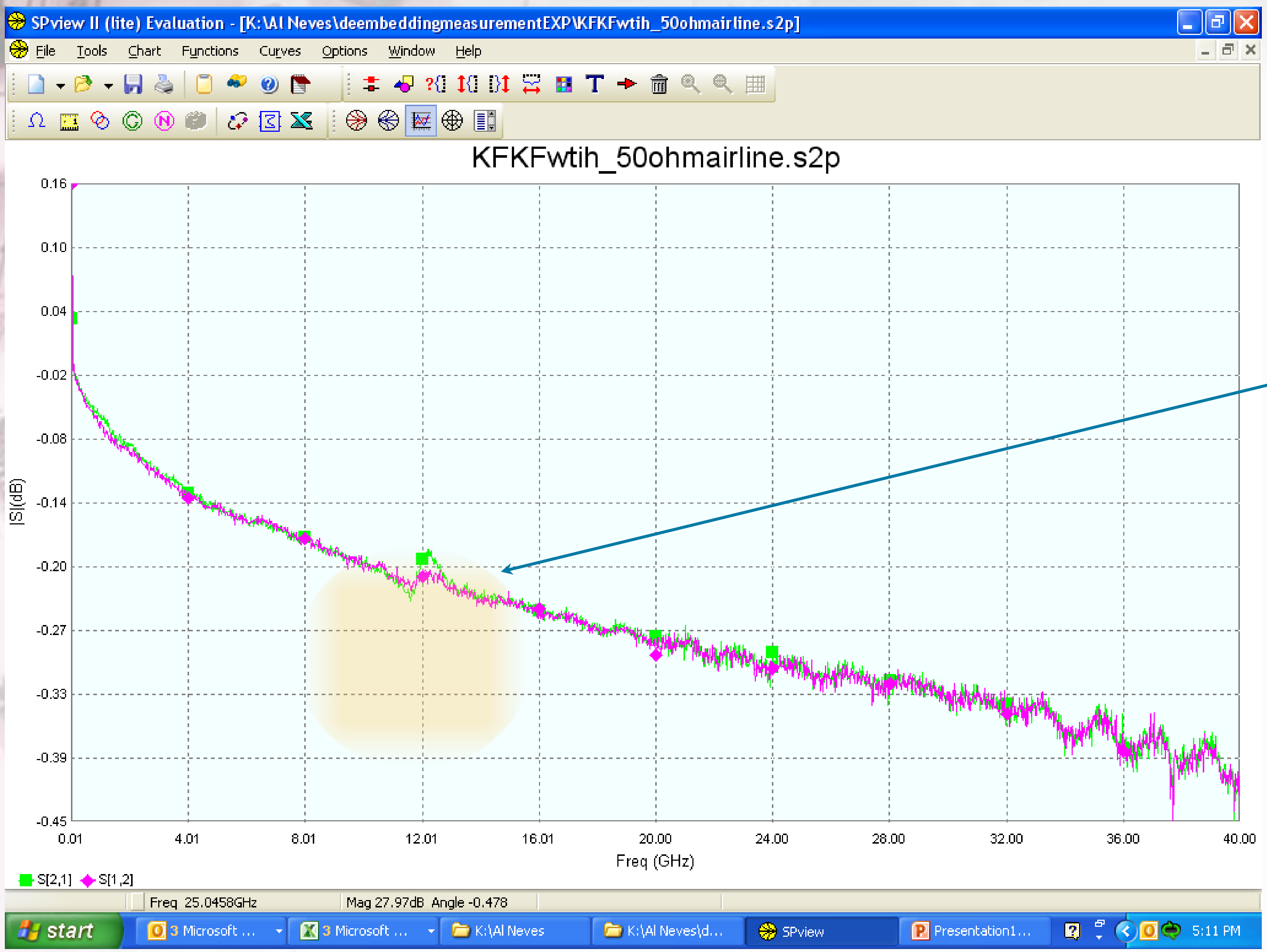
Good S-parameters start with Good Calibration! Simple Cal Verification

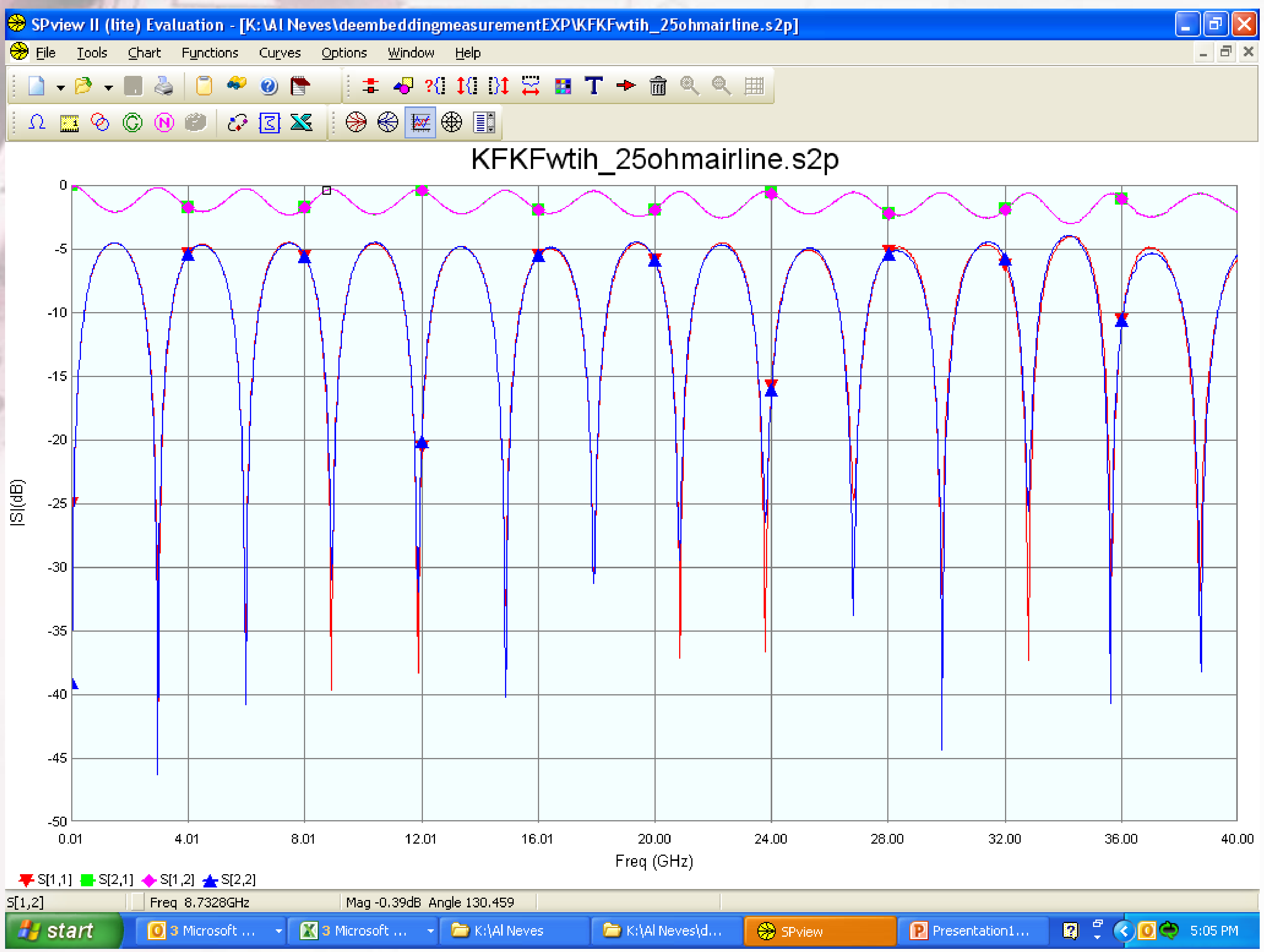


Cal verification using precision airlines
First, examine transmission aberrations, then return loss mag



I may check this S21 with no calibration enabled

Resonant structure like Beatty Standard are excellent for calibration validation



This Structure has obvious, out to 40GHz:

1. Symmetry
2. Reciprocity
3. Low Distortion/abberation
4. High Dynamic range

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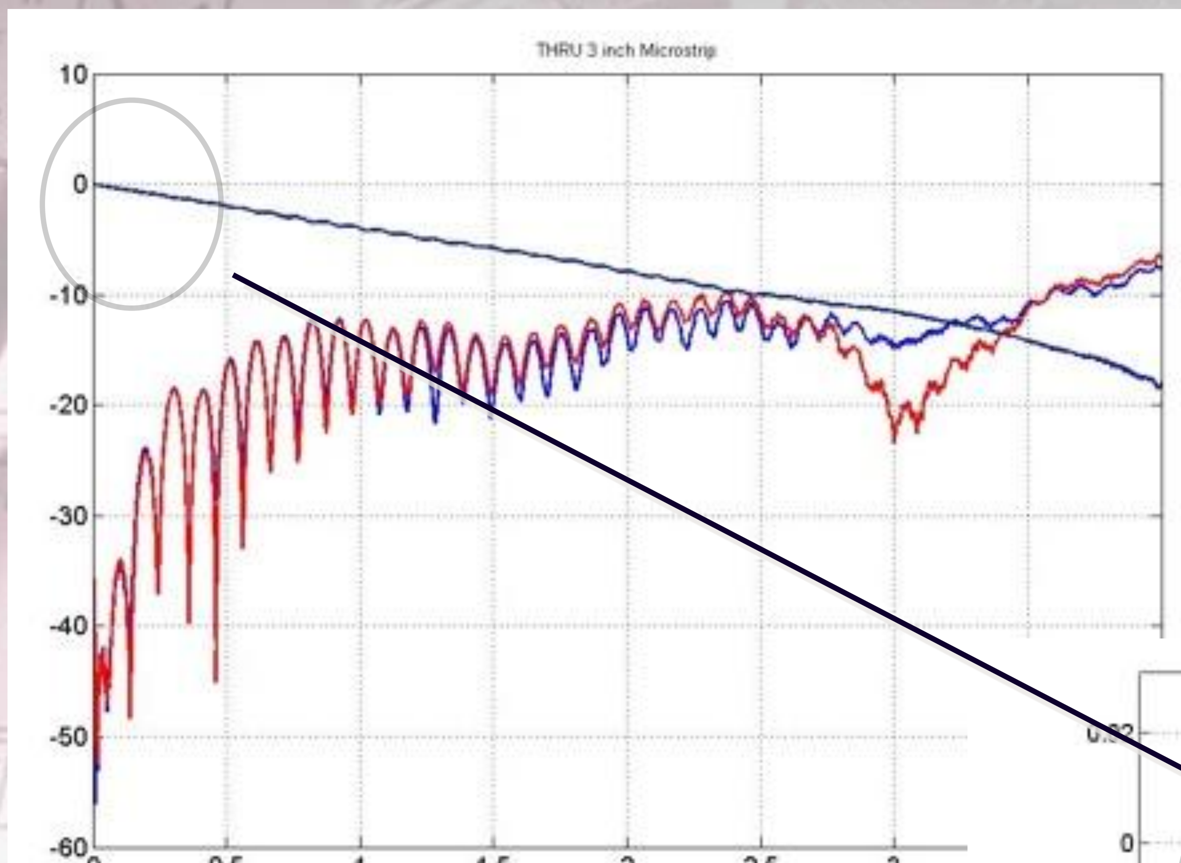
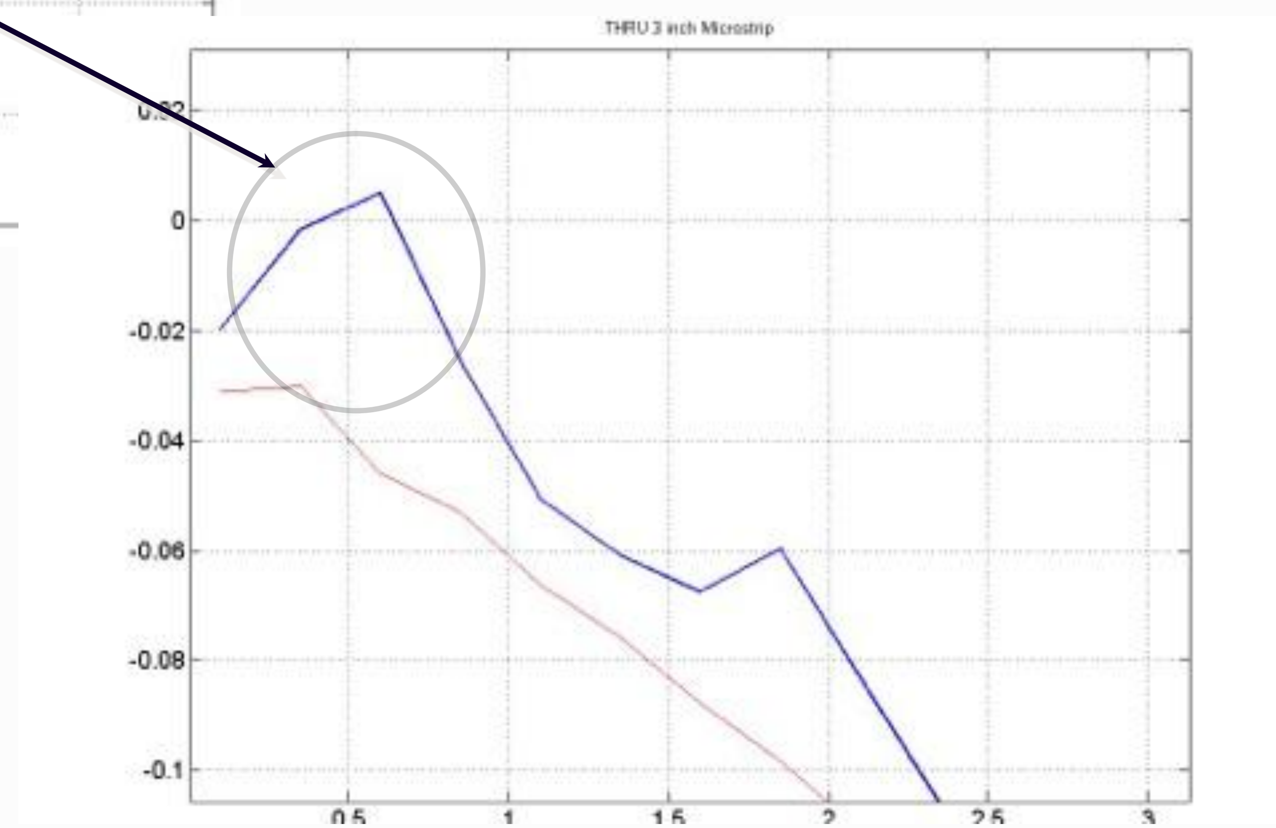
Example of Simple THRU for TRL:

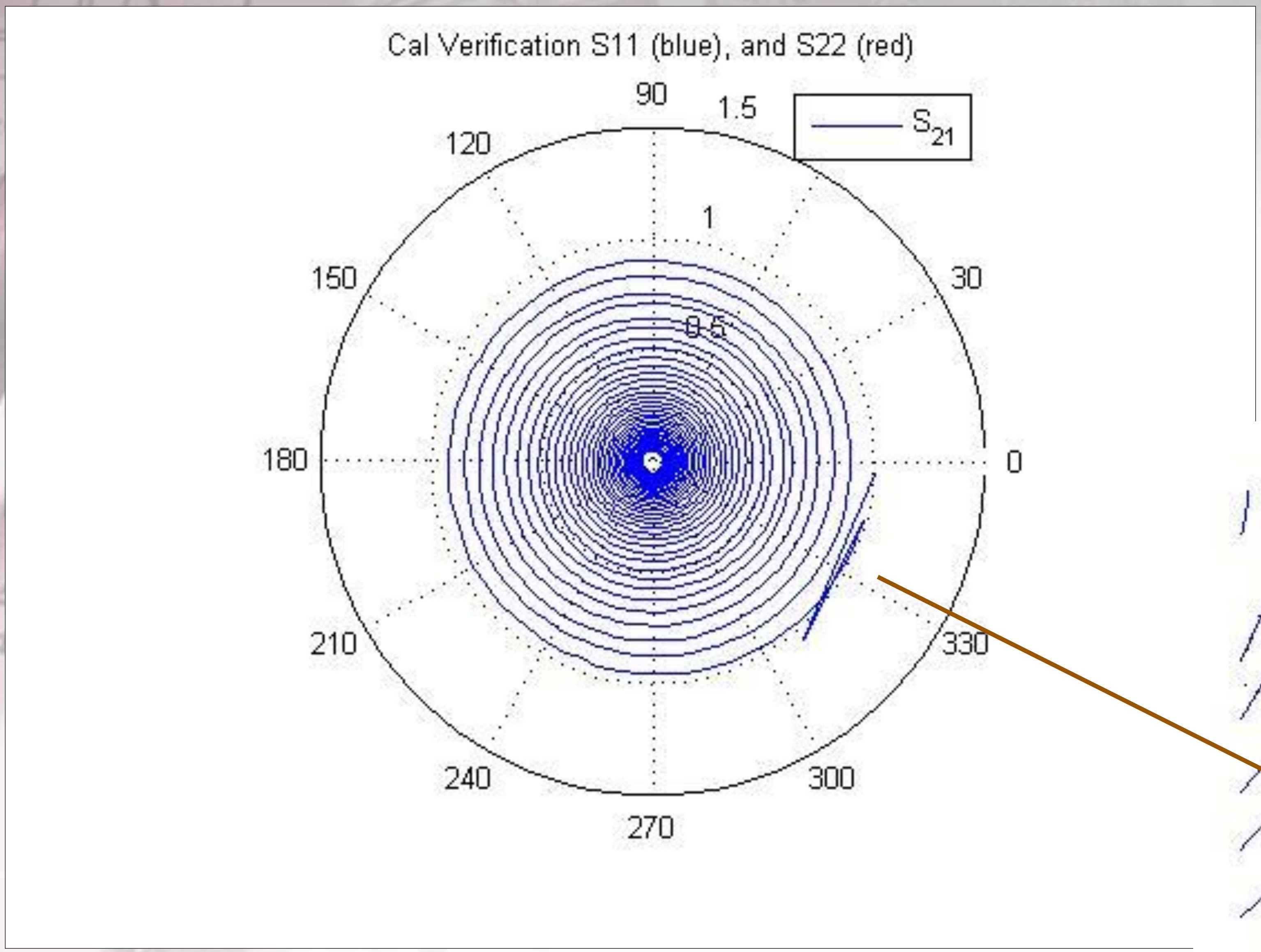
Simple check of obvious Passivity Violations. The check of |S21|>1 is NOT sufficient however!

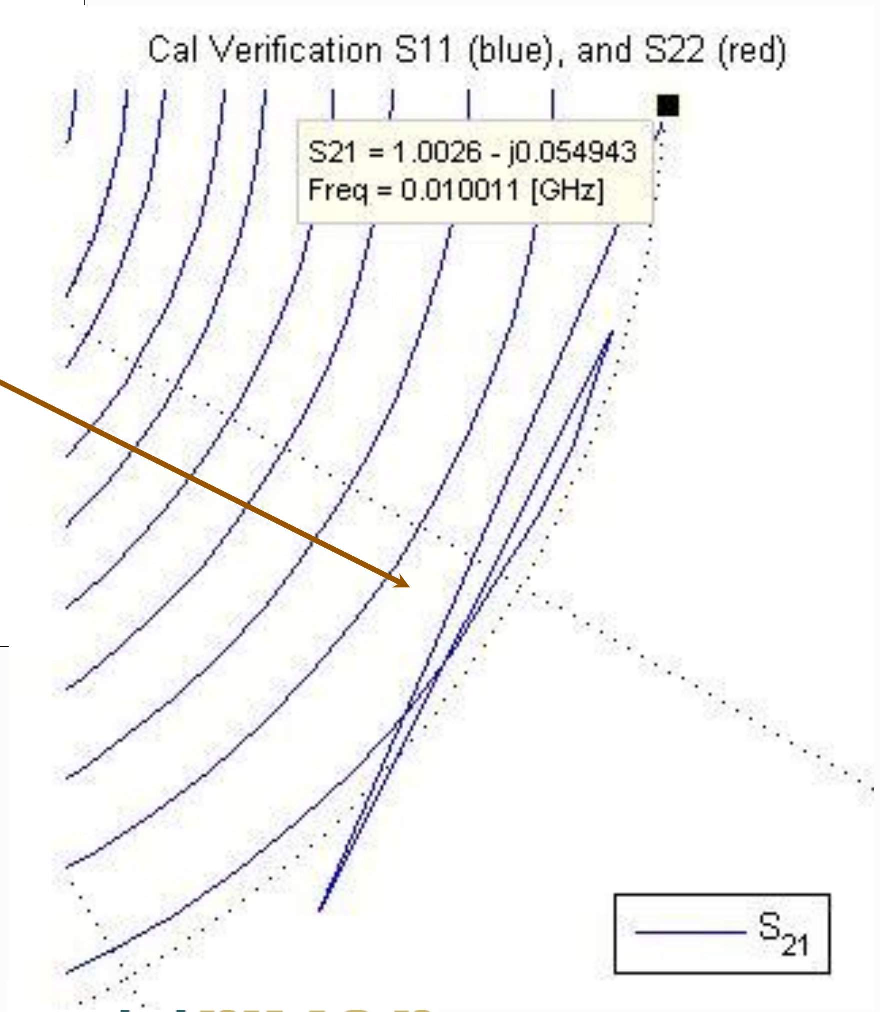


Another example using on-board THRU



Analysis of Calibration Causality Using Polar Plot, Causal S-parameters should only rotate clockwise





Quick Polar view of Insertion locates non-causal behavior

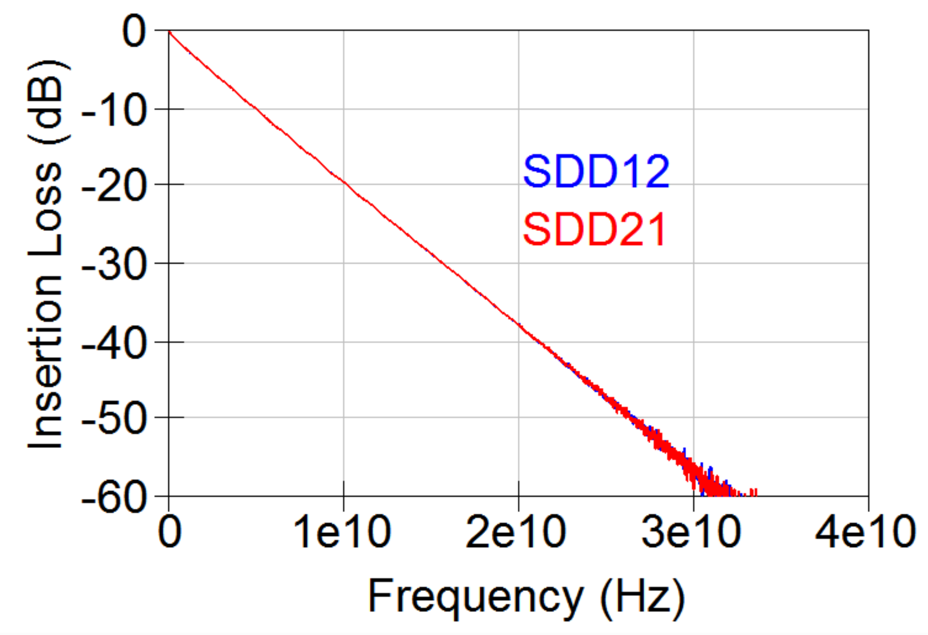
Now, lets discuss Data - Mining....

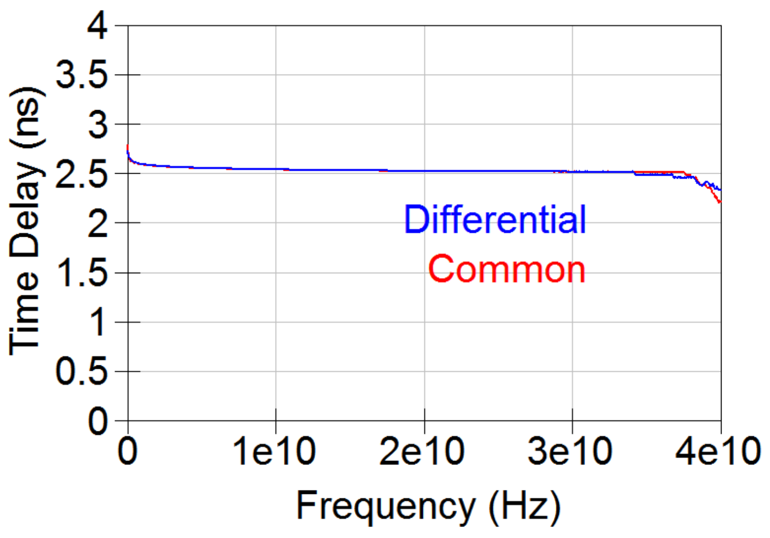
Data Mining the S-parameter Models

- S-parameters are too often treated as a “black box”
- Step 1 of the method: build an S-parameter library
- Data-mine your library learn all you can about your models
- Five parameters are of particular interest:
  - Differential return loss
  - Differential insertion loss
  - Differential time delay
  - Common time delay
  - Mode conversion terms

Mining Differential & Common-signal Insertion Loss

- From SDD12 & SCC12 (or other IL S-params), predict/measure:
  - Channel bandwidth
    - Ex. -10db @ 5GHz
  - Time delay through channel
    - 2.5 ns nominal, TD vs. frequency shows dispersion
  - Loss estimate
    - Slope: 2dB / GHz / 11in, or 2dB / GHz / 2.5ns
  - Overall S-param quality (via comparison to SDD21 and SCC21)
    - Extremely close match





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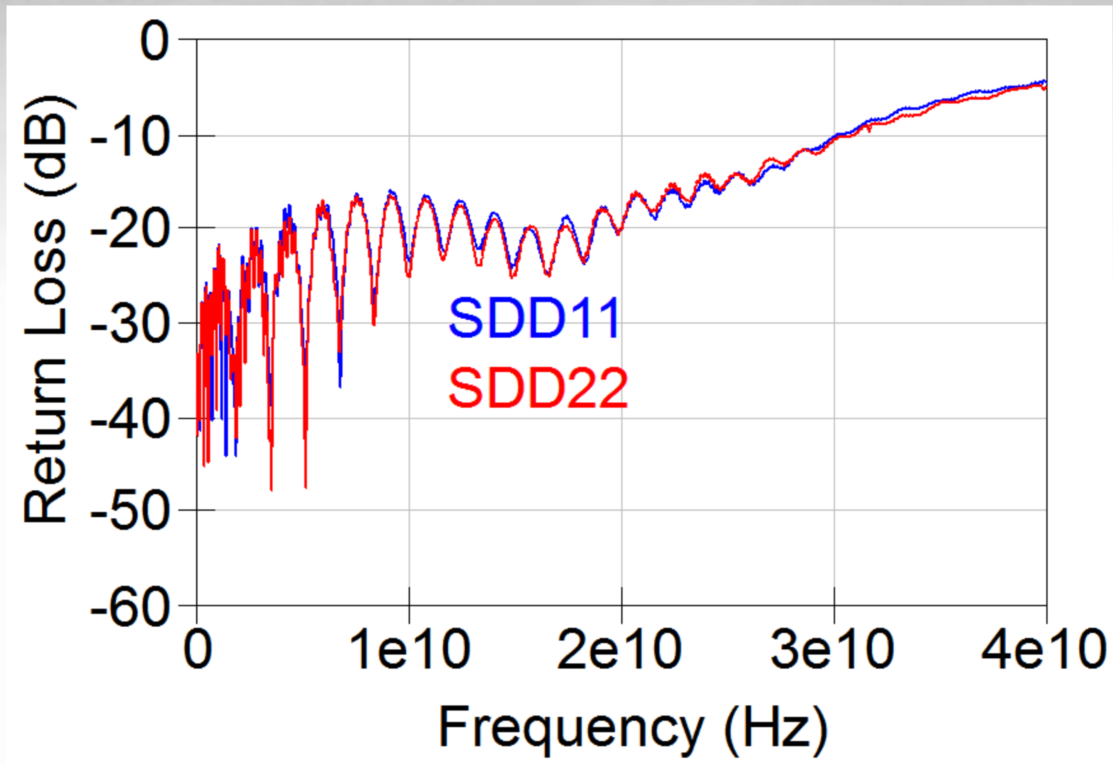
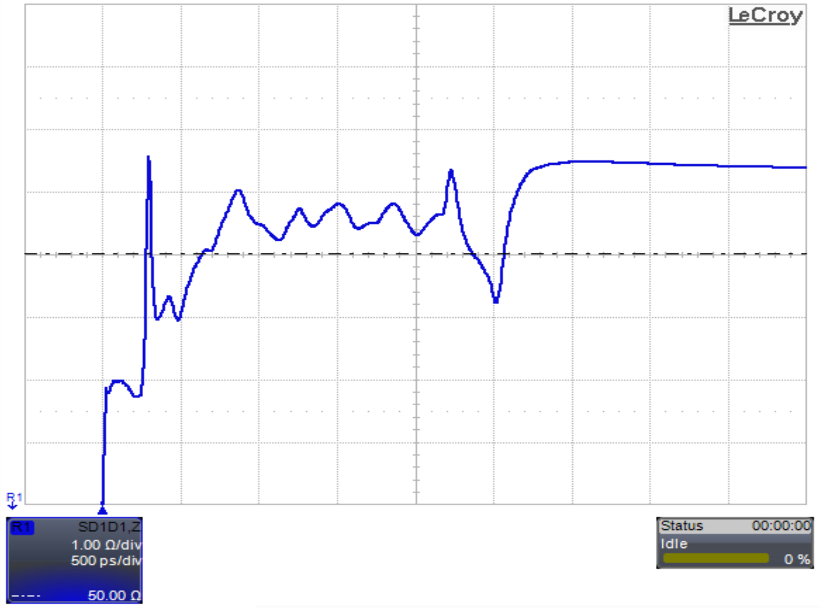
Mining Return Loss S-parameters

- Frequency domain:
  Ripple is evidence of mismatches
  - DUT/port impedance mismatch
  - Trace/Launch mismatch



- Convert to time domain to:
  - Calculate impulse, step response
  - Calculate impedance profile, rho
  - Understand local variations from nominal impedance
  - Spatially locate unexpected impedance mismatches



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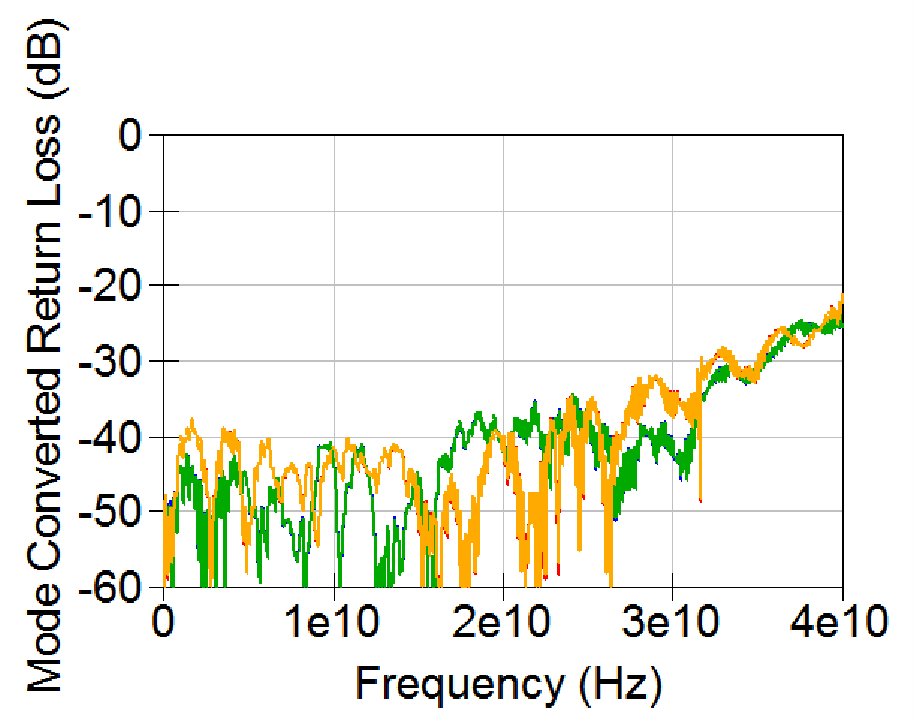
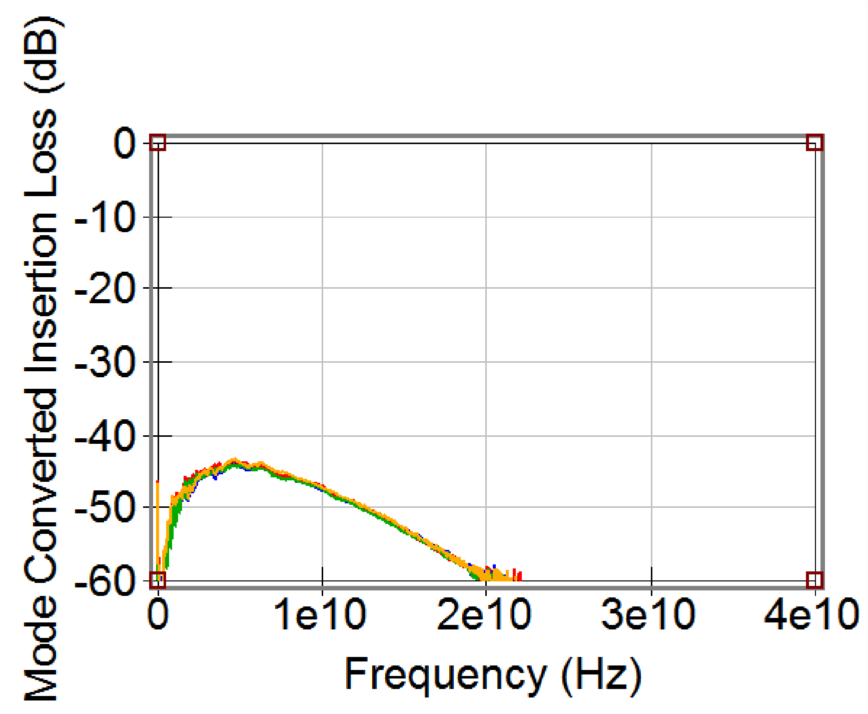
Mining Mode Conversion S-parameters

- SDCxy and SCDxy is a result of differences between + and – nets
- Conversion from Differential to common causes latching issues





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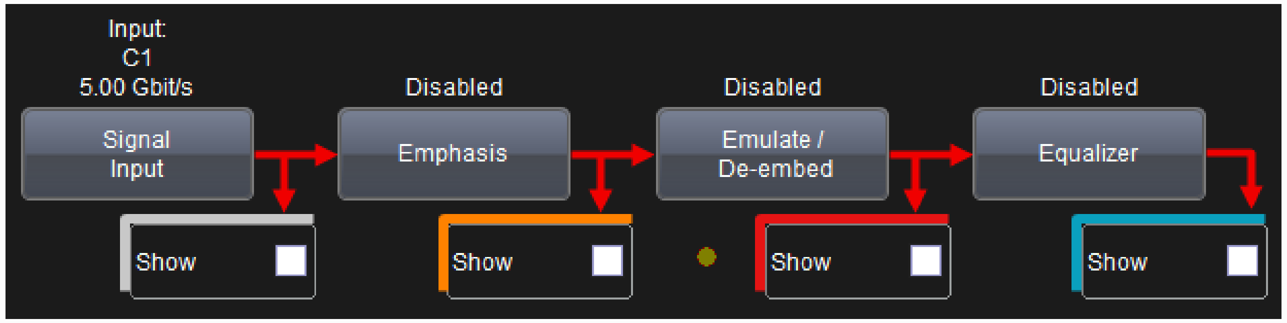
Step II of the Method – Equalization Analysis

- Understand the signal integrity impact of the S-params
- Tools are available to simulate eye:
  - LeCroy Signal Integrity Studio
  - Agilent ADS
  - MATLAB
- Goal: determine what is required to open the eye
  - Transmitter emphasis
  - CTLE
  - DFE
  - FFE



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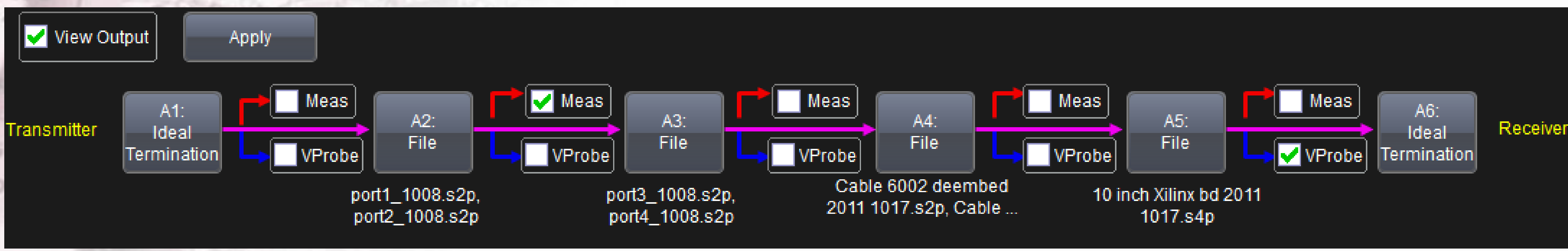
Dealing with fixtures

- Tools are also available to calculate waveforms at any point in your circuit or to remove effects of fixtures
  - Example: LeCroy EyeDoctor / VirtualProbe



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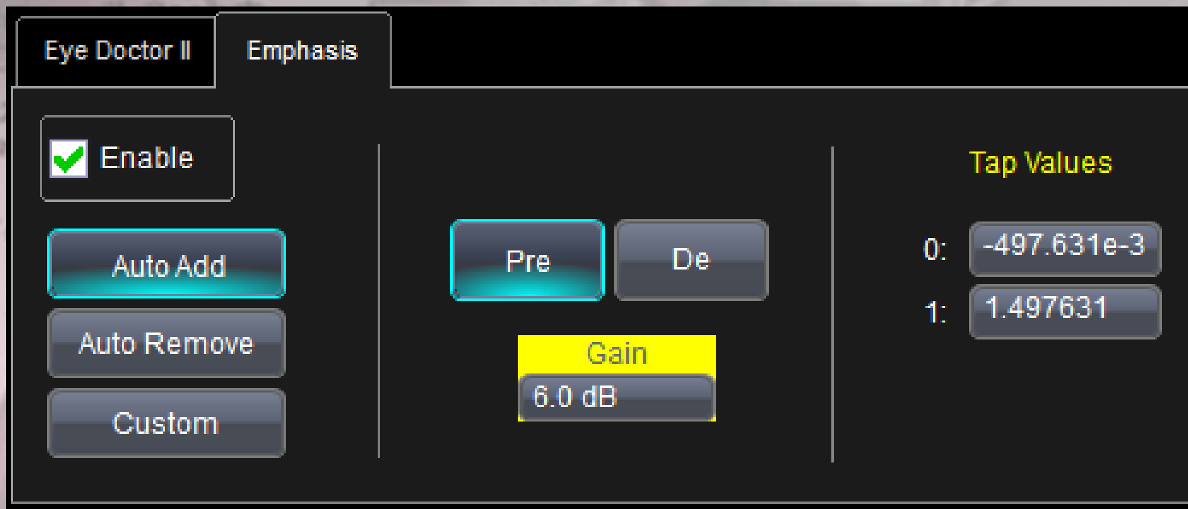
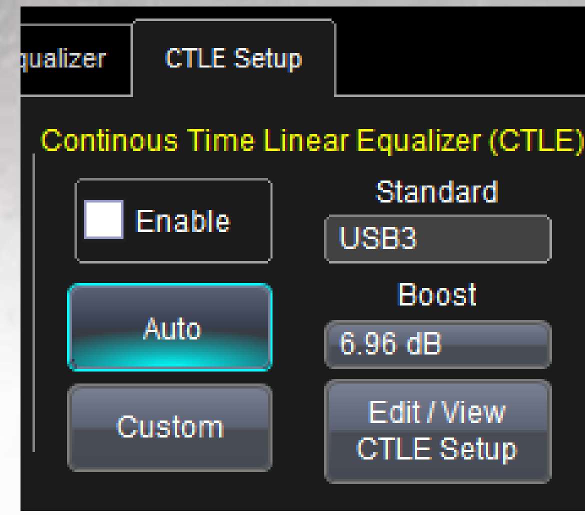
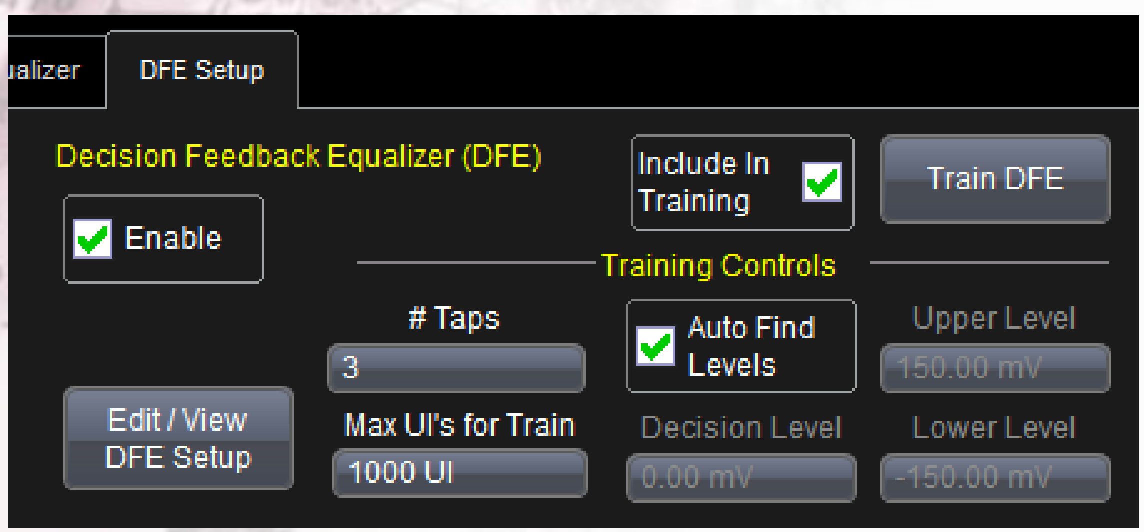
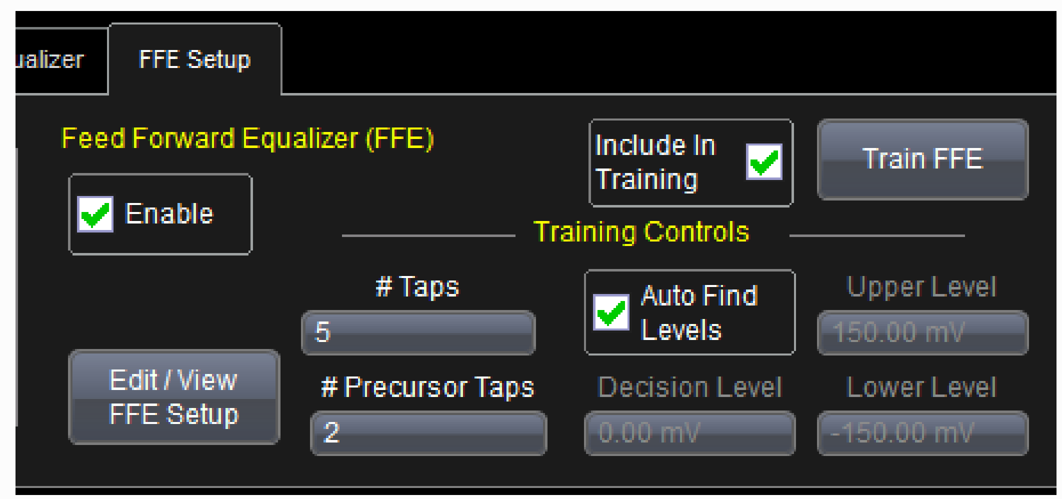
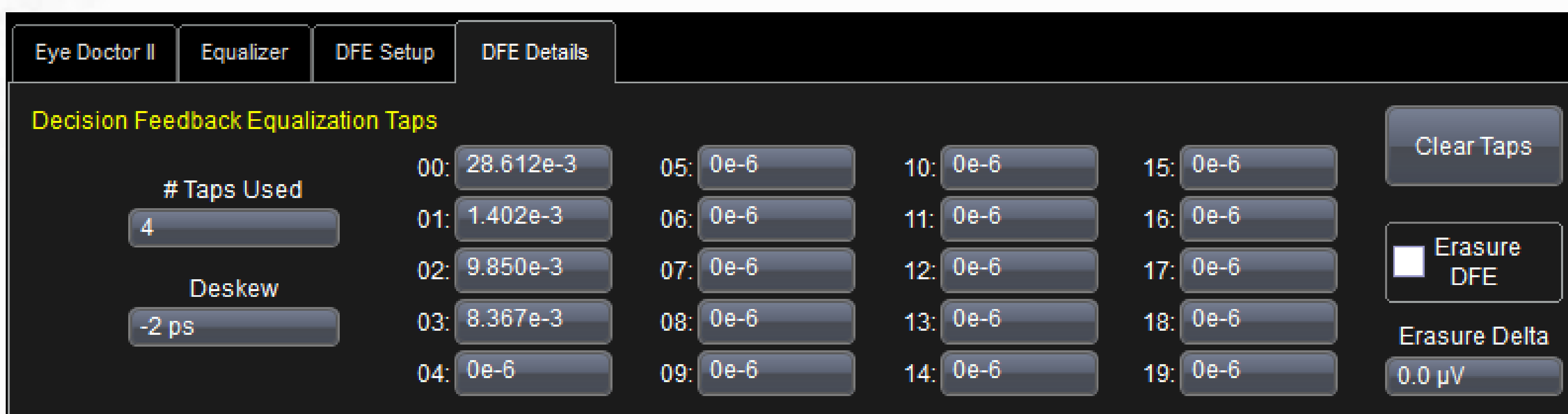
Equalization Techniques

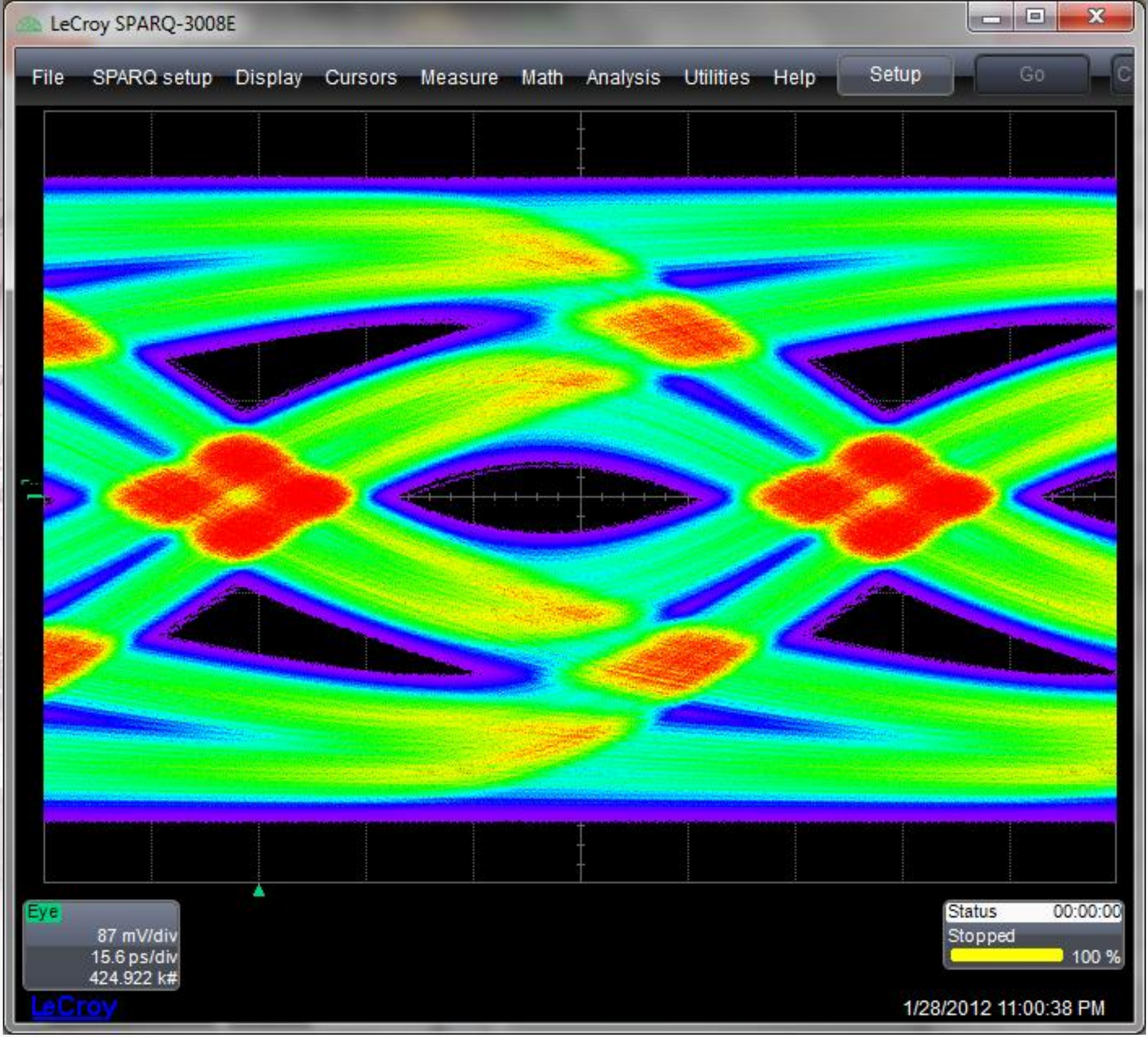












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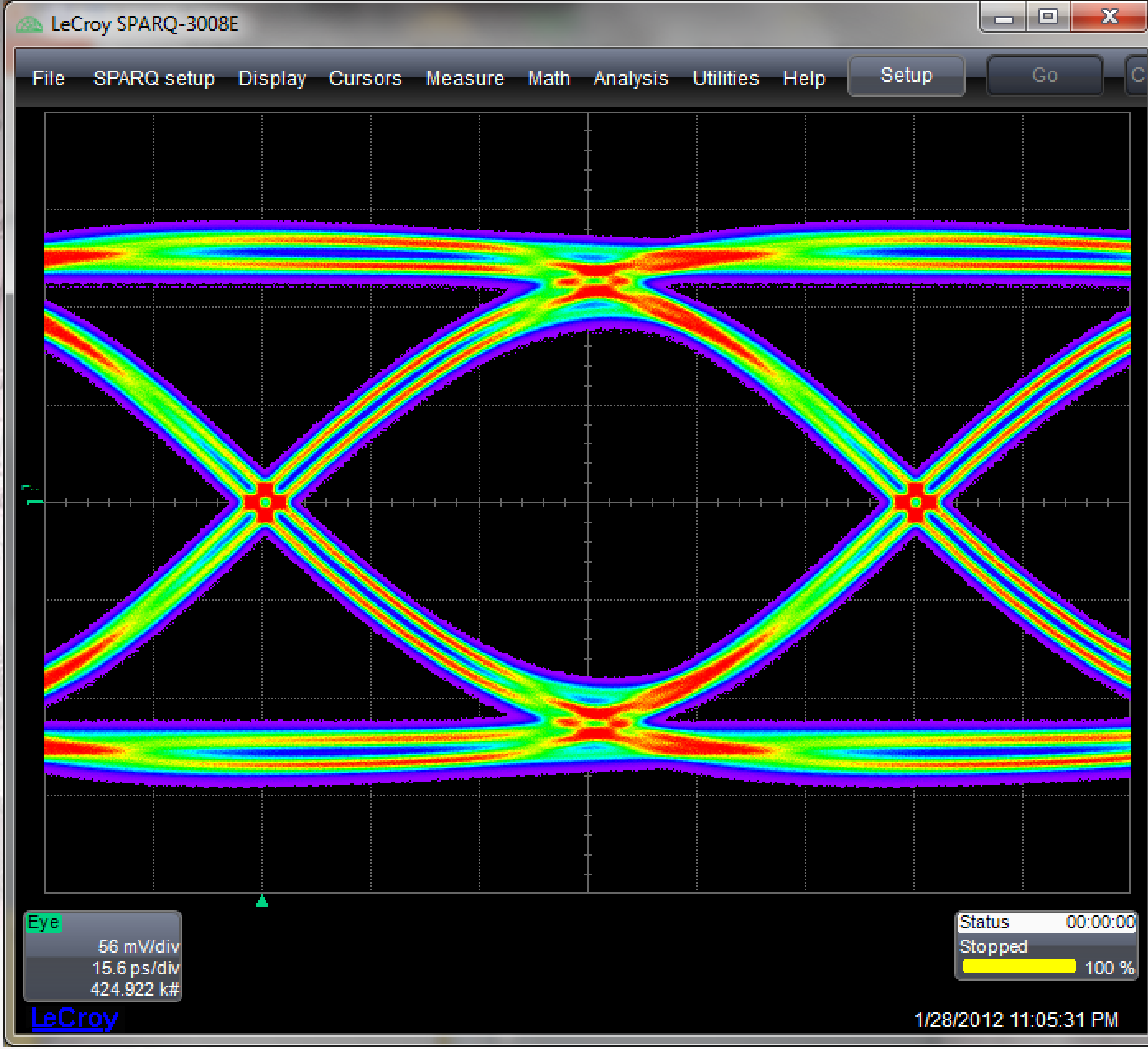

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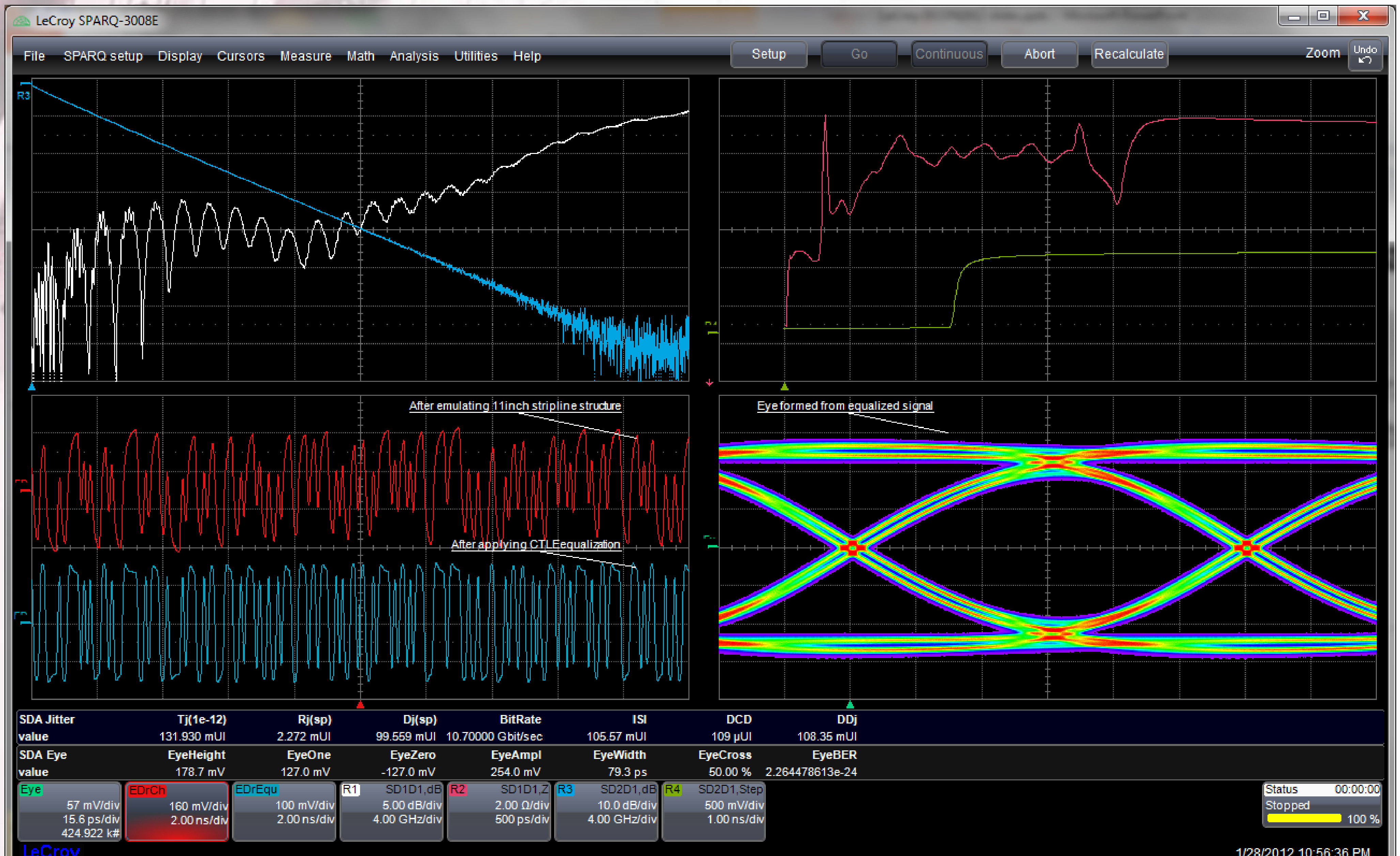
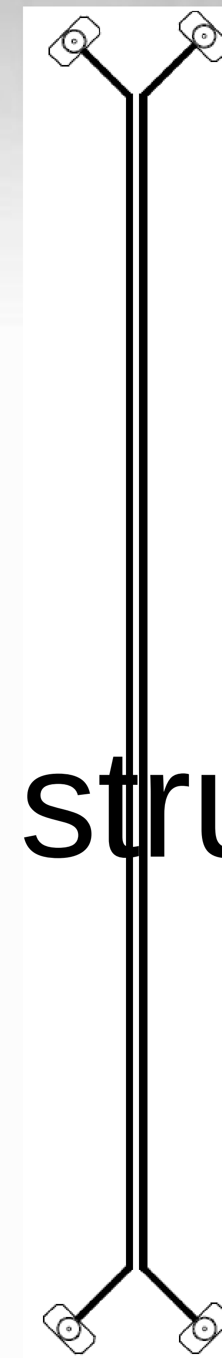
Example Analysis – 11” structure

Simultaneously view S-parameters, signals before/after equalization @ receiver, eye and jitter analysis





11” structur

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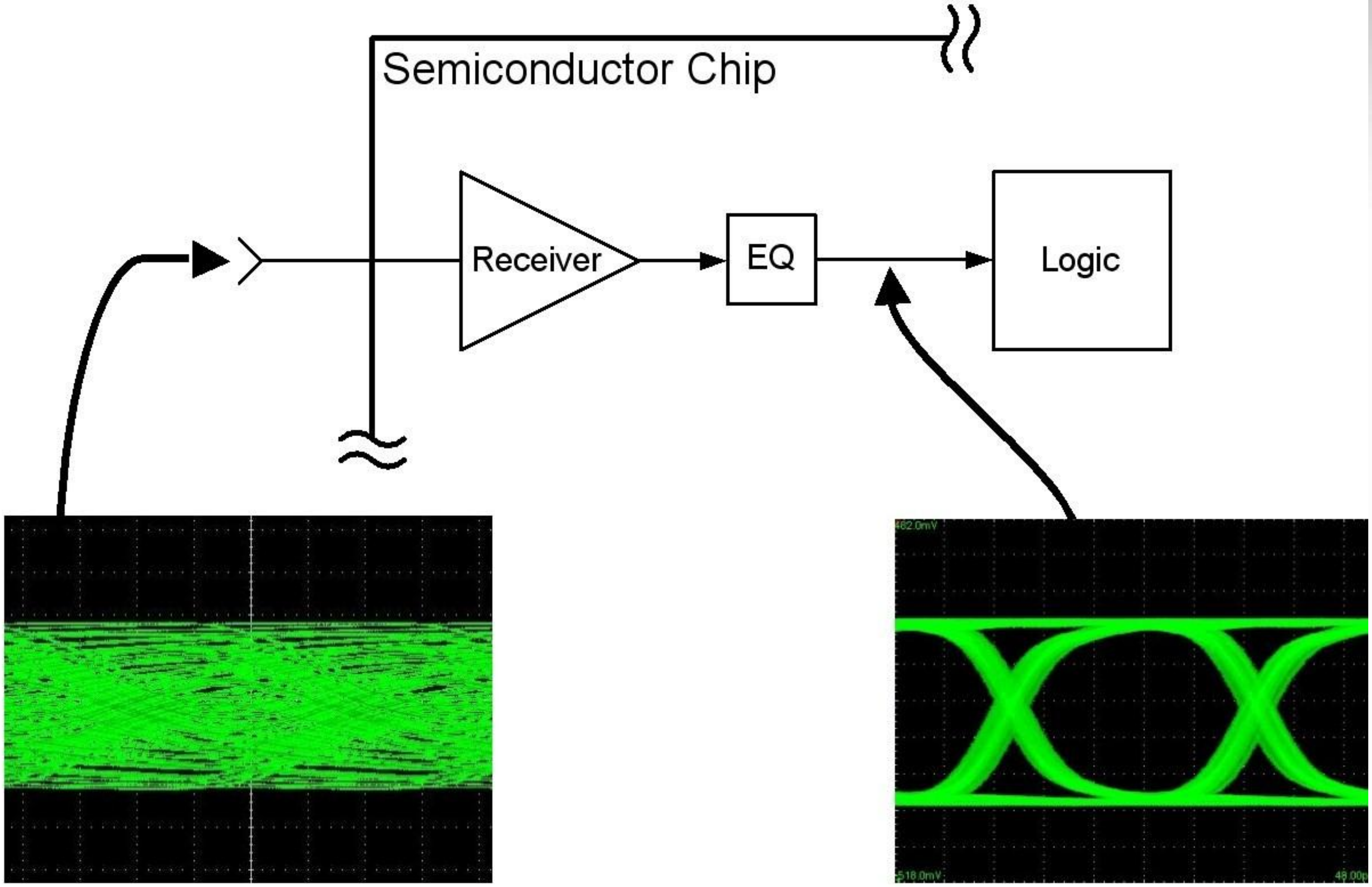
Equalization in light of Crosstalk

- While losses increase with frequency, isolation decreases with frequency
- FFE and CTLE either maintain or increase the SNR
  - Amplify higher frequencies relative to lower frequencies to compensate for channel losses
  - This in turn amplifies or enhances the high frequency crosstalk
- DFE leverages its decisions back to the input of its equalization filter
  - SNR increases w/ “clean” decisions fed back
  - Depending on channel and noise characteristics, the DFE can provide at least 2 dB of output SNR improvement over CTLE and FFE equalization

System Designers Are Going Blind



Signal arriving at input with severe high-frequency attenuation effects.

Signal input to logic circuit after internal equalization.

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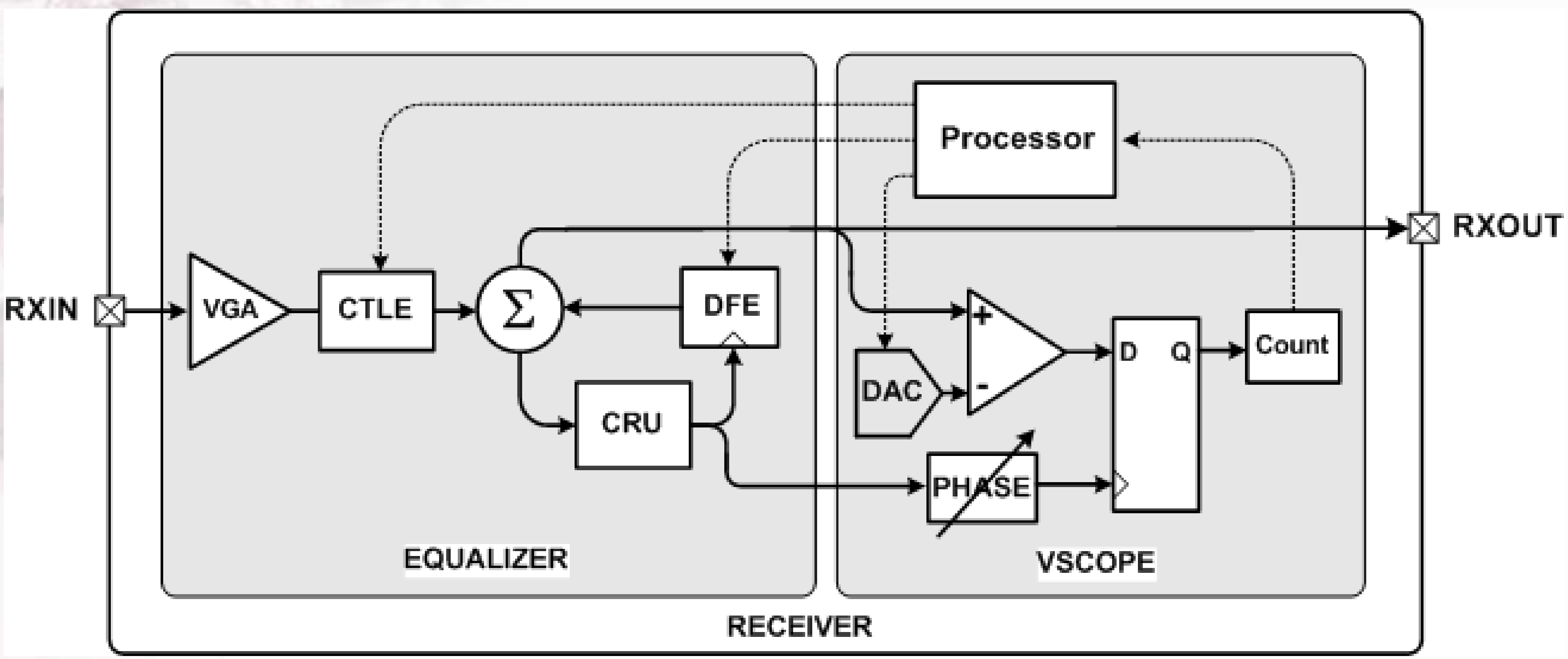
Embedded Waveform Viewing – Equalizer Modes

- Unity Gain Mode - set equalizer to unity gain
  - DFE contributions = 0, CTLE to Flat frequency response and VGA gain =1
- Link Monitor Mode - processor drives CTLE and DFE positions
  - VScope inner eye height is key metric



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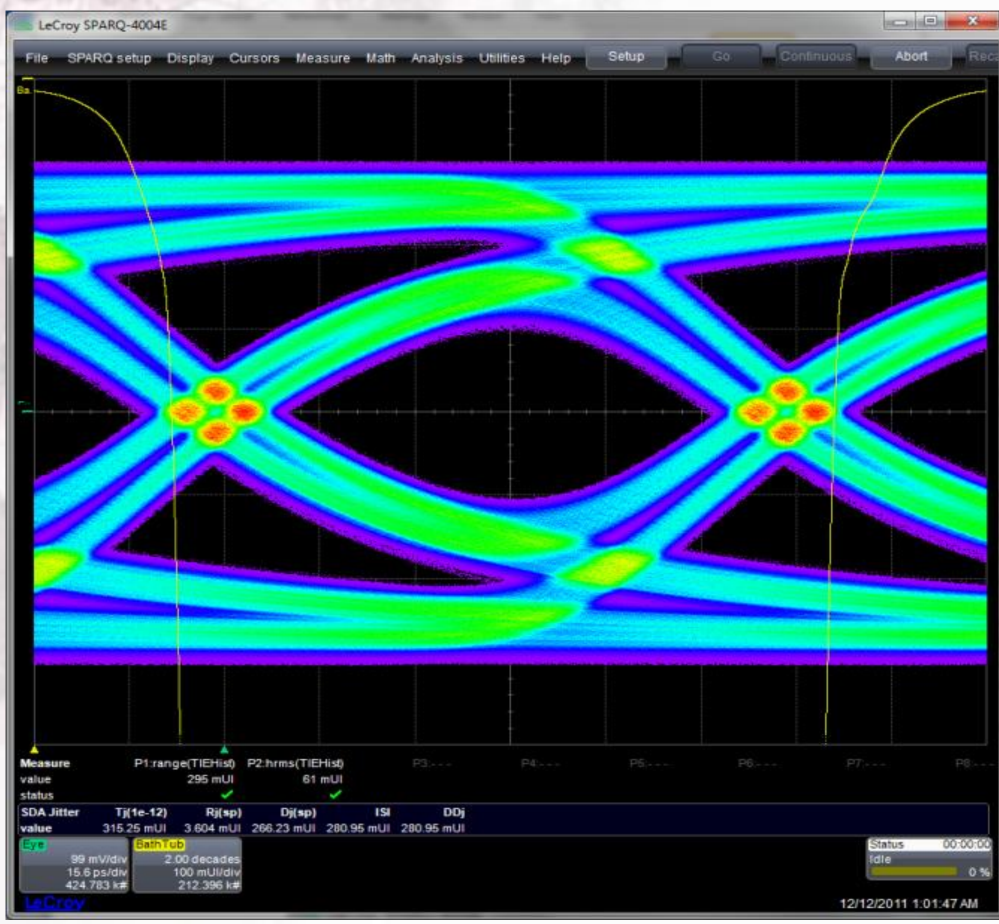
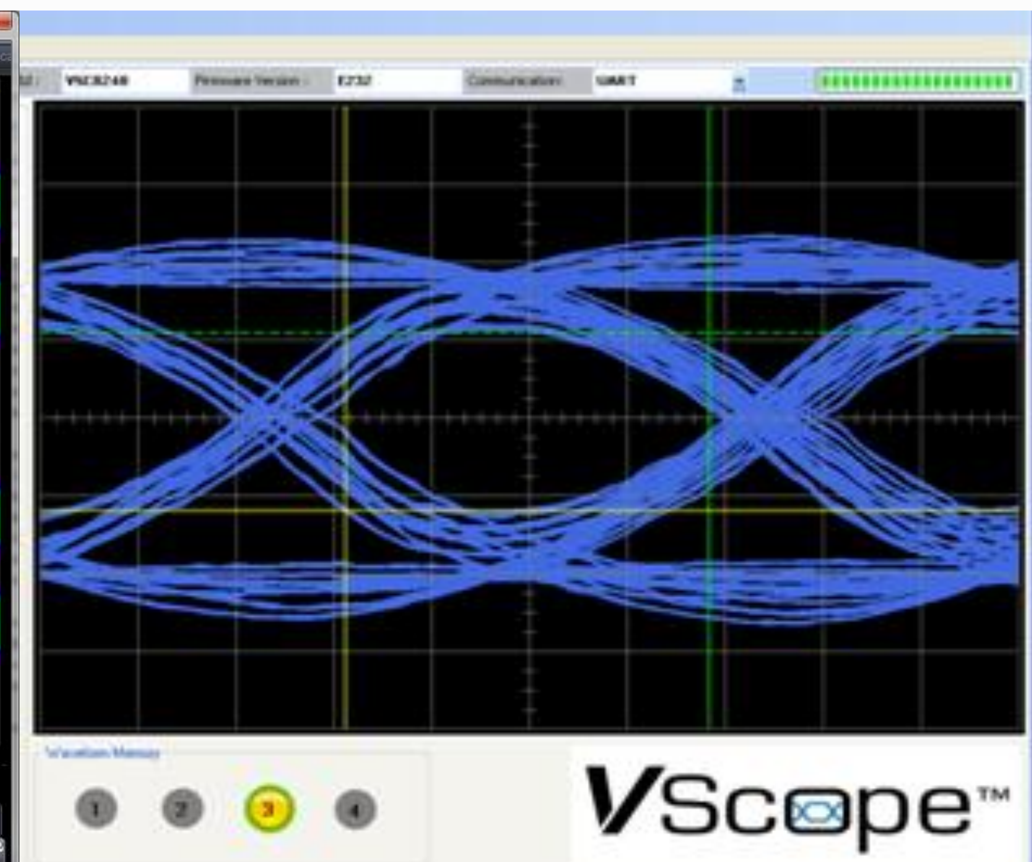
The VScope to Simulation Comparison

- "Scope" Unity Gain Mode is remarkably similar to what the simulation produces
  - Key landmarks (inner eye height and width) are visible
  - The voltage/phase resolution and sample time/thresholds determine the ability to see individual edges





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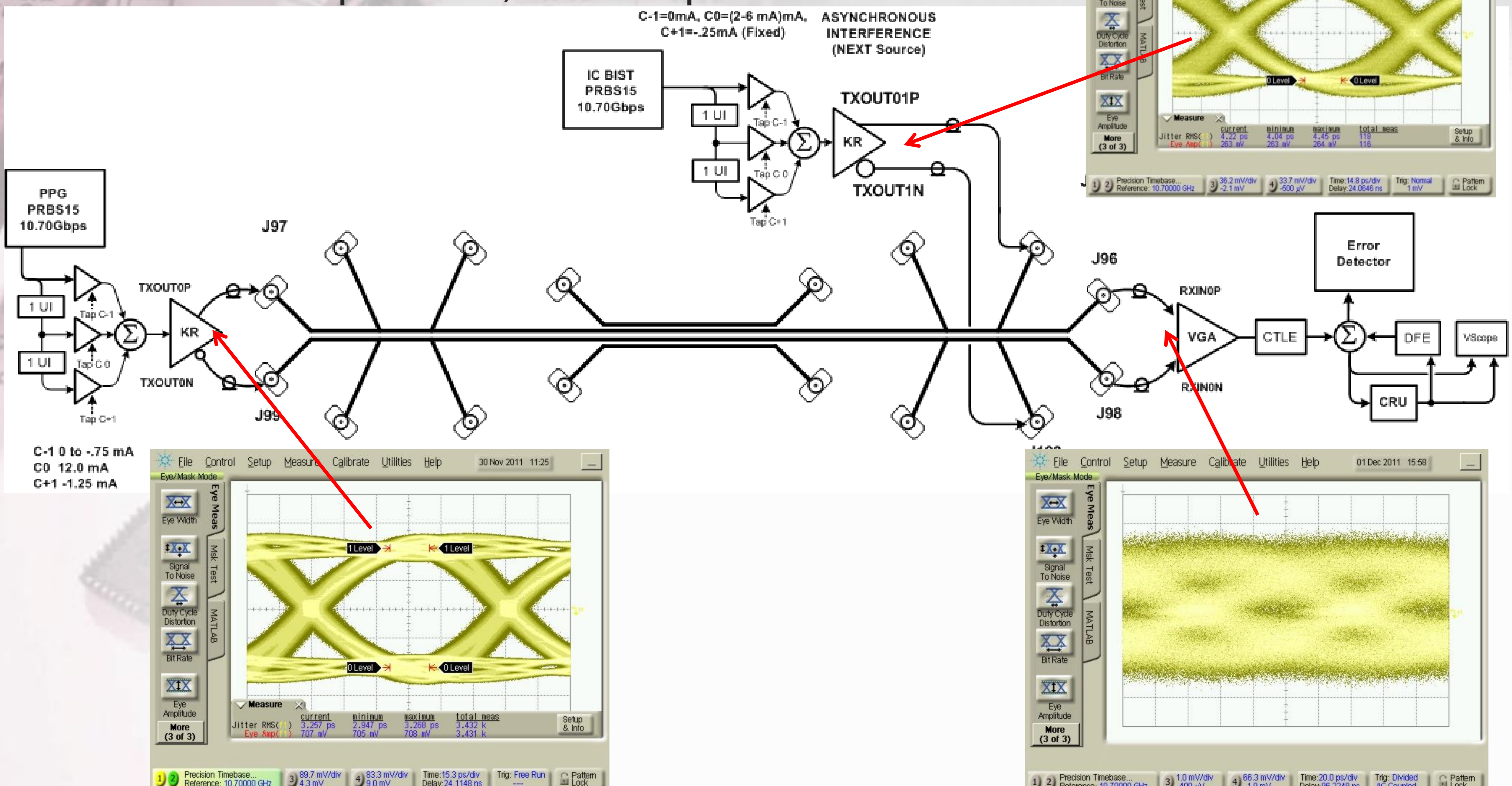
CrossTalk Environment Block Diagram

- 16 Port test platform, unused ports terminated



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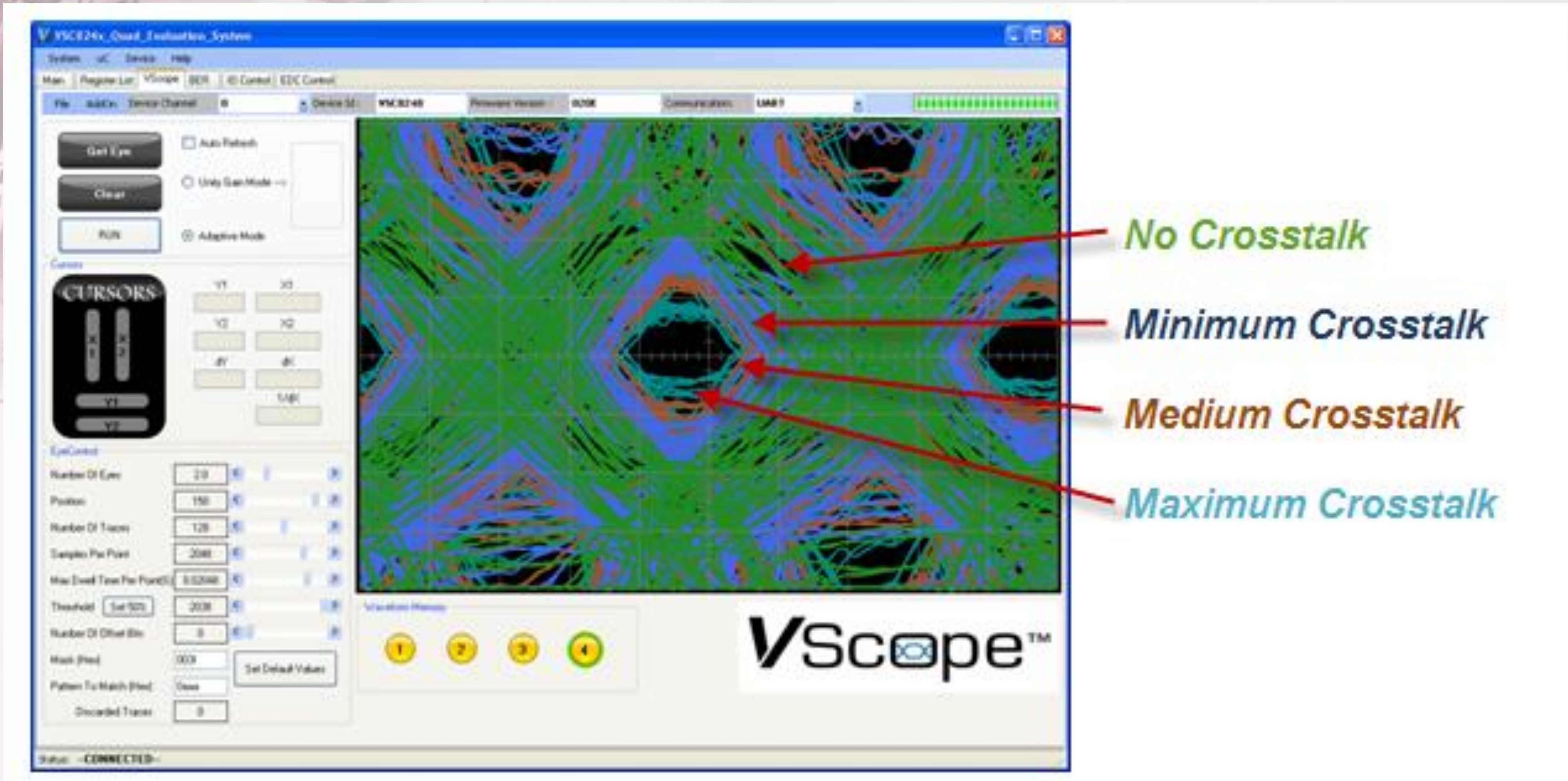
VScope and NEXT Level Resolution

- Three levels of NEXT show measureable differences in inner eye height
  - Enables receiver equalization filter adjustment



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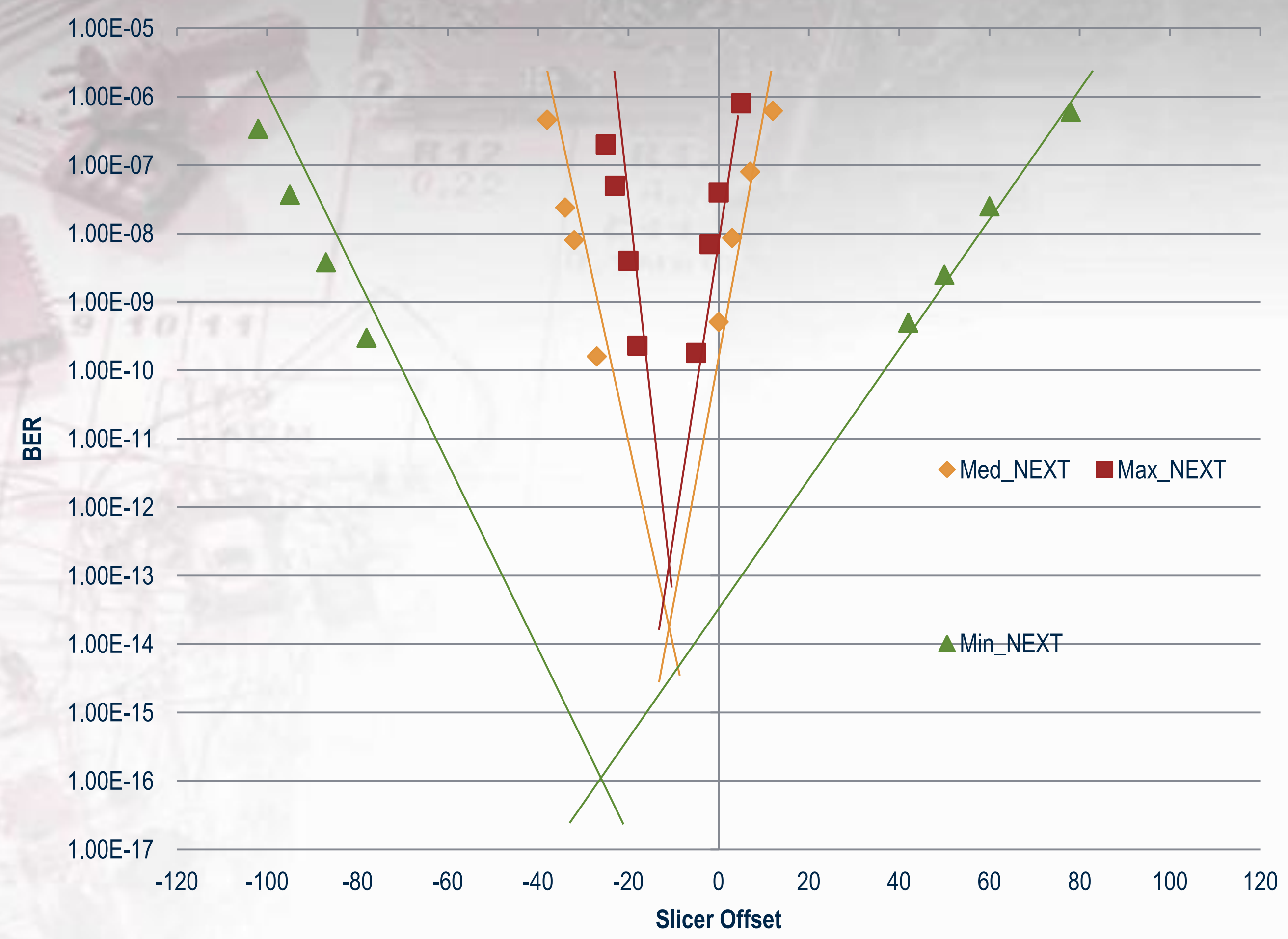
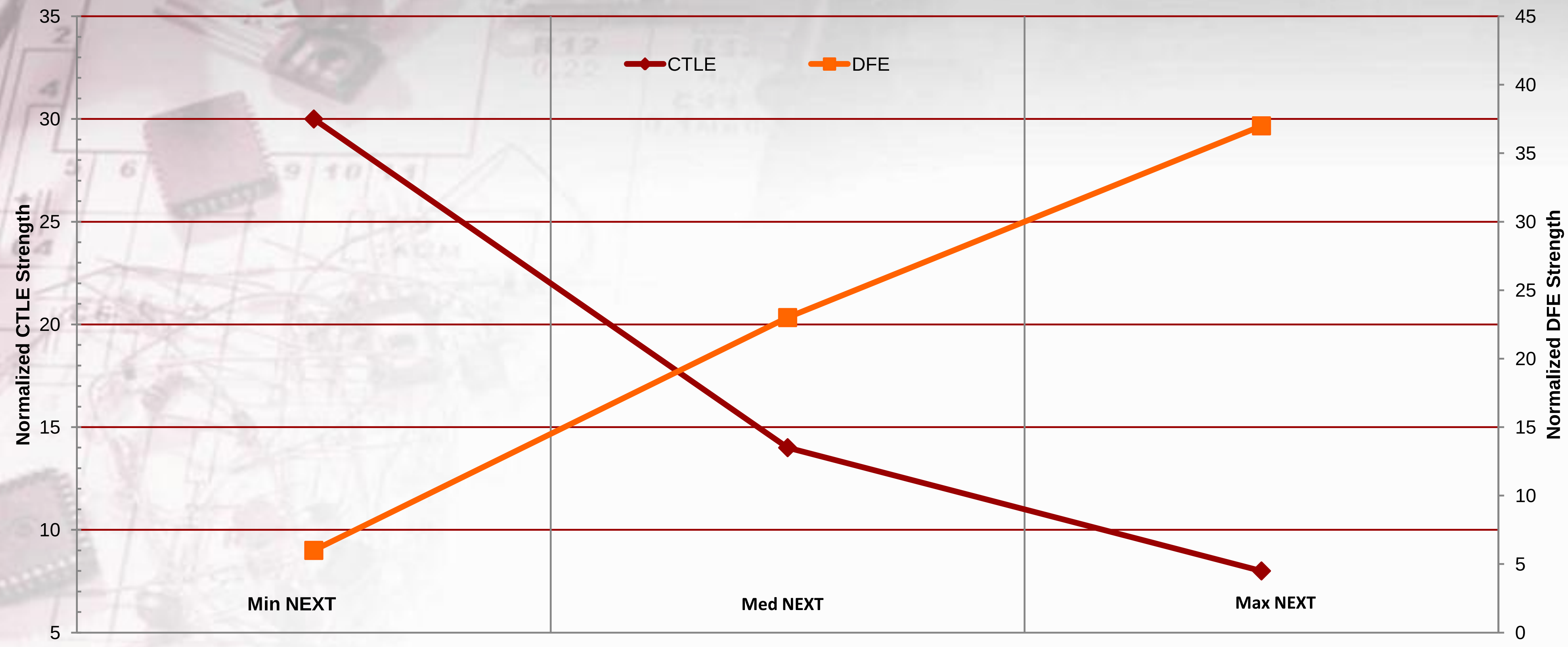
System Margin vs. NEXT Levels



Trial	NEXT Level	CTLE (EQ Strength)	DFE (EQ Strength)	Voltage Margin @ 1e-12 BER (mV)
1	Minimum	30	6	70
2	Medium	14	22	16
5	Maximum	8	37	5

CTLE and DFE trading off EQ strength



- In the face of different levels of crosstalk, the CTLE and DFE trade-off equalization strengths
- More DFE is required to combat SNR in Max NEXT environment

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BER-V Margin Improvement w/ more DFE

Trial	NEXT Level	CTLE (EQ Strength)	DFE (EQ Strength)	Voltage Margin @ 1e-12 BER (mV)
3	Maximum	30	6	0
4	Maximum	14	22	0
5	Maximum	8	37	5

- Table compares 3 sets of CTLE & DFE equalization settings in Max NEXT Level environment
- Trading off CTLE for more DFE equalization shows Voltage Margin improves from no margin

Crosstalk Mitigation Conclusions

- The methodology enables crosstalk aggressed test environments that can lead to better equalization trade-offs
- Embedded waveform views provide a useable metric for optimizing the equalizer
- DFE equalization improves SNR, better than FFE or CTLE
- Equalizer performance in the presence of crosstalk is improved with increasing DFE strength and decreasing CTLE strength

Future Work

- Quantify the NEXT environment by analyzing 16 Port S-parameter data for the test platform - Insertion loss to Crosstalk Ratio (ICR)
- Investigate impact of different NEXT Transmitter frequency responses (PRBS lengths for example)
- Optimize Filter tuning algorithm using additional VScope metrics