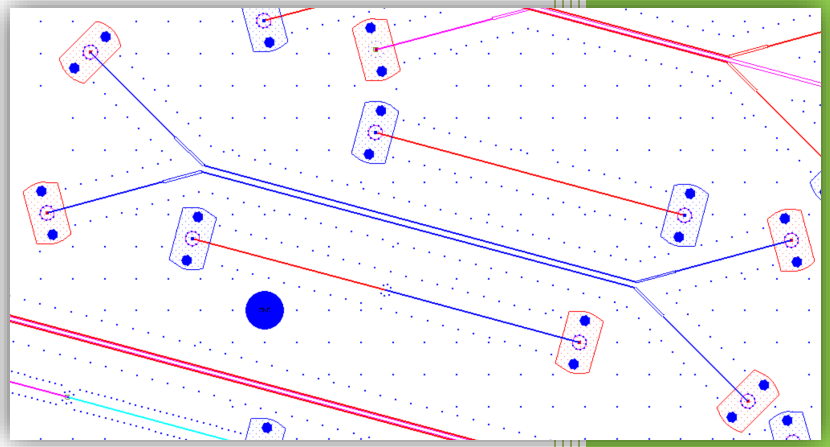
+50GHz, 56-112G PAM-4, Thoughts and Opinions For Designing Stellar S.I. Test Fixtures

Alfred P. Neves
Chief Technology Officer
503 679 2429
al@wildrivertech.com



The Challenges of +50GHz SI

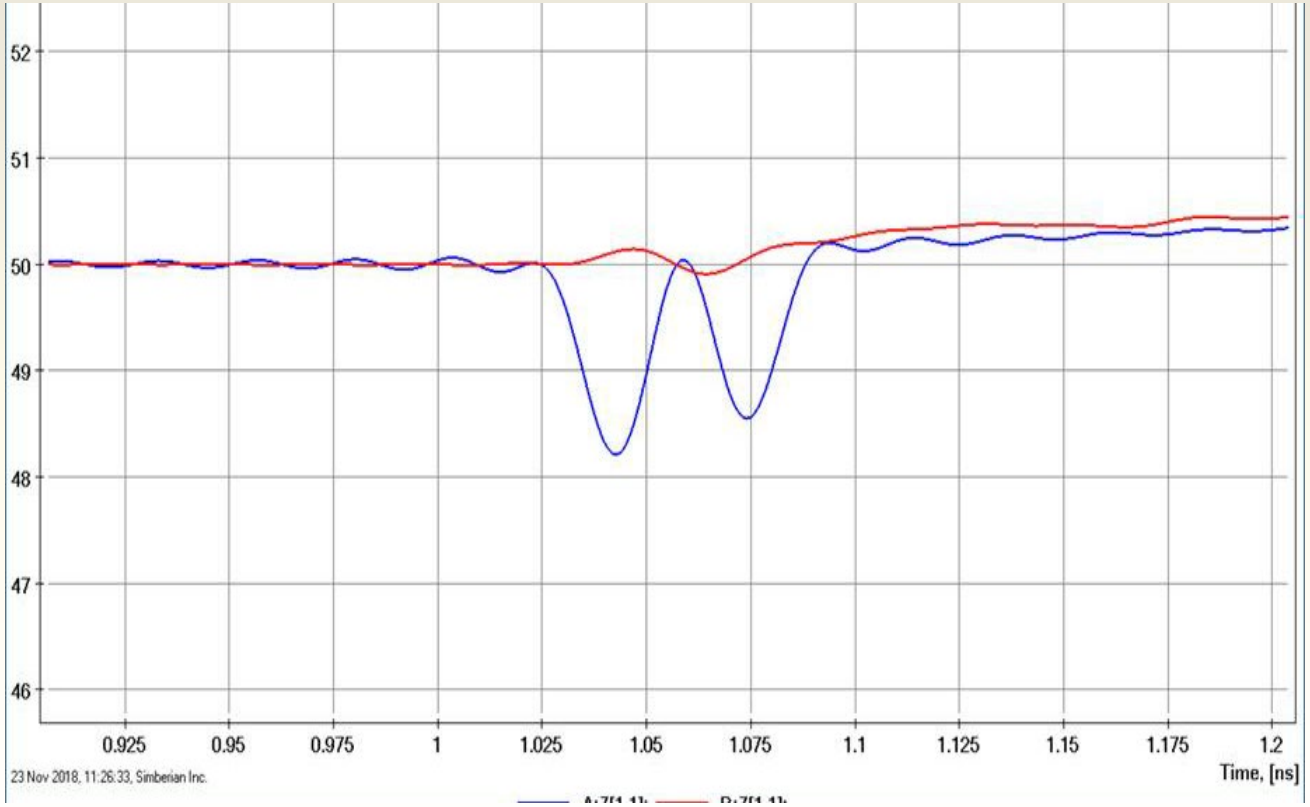
- EDA Tools and Simulation Methodology
  - Benchmarking the tool
  - Methodology and Tuning Your Simulation
- What Exactly is Good SI?
  - The answer is not always obvious
  - IEEE P370 TG1
  - How many spins to get there?
- The “Alamo Strategy” for Test Fixture Architecture
  - The Tale of 2 Titanic Captains
  - Always have a way out, the “Alamo Strategy”
- The “Fabrication Hurdle” What is it, how to get past it
- New Paradigm for Critical SI Connector Vendor Working Relationships
- Why Program and Project Management gets in the way of 70GHz SI
  - Schedules versus Innovation and Building Technologies
  - Concurrent EDA Teams
- Closing Ideas
- Conclusion
- Open Discussion

SI Technologist Mindset:

- *Paranoid*
- *Always thinking of what can go wrong, how to mitigate*
- *Always innovating for future challenges*
- *DesignCon+conferences, investment, takes career risks*

Captain Edward J. Smith

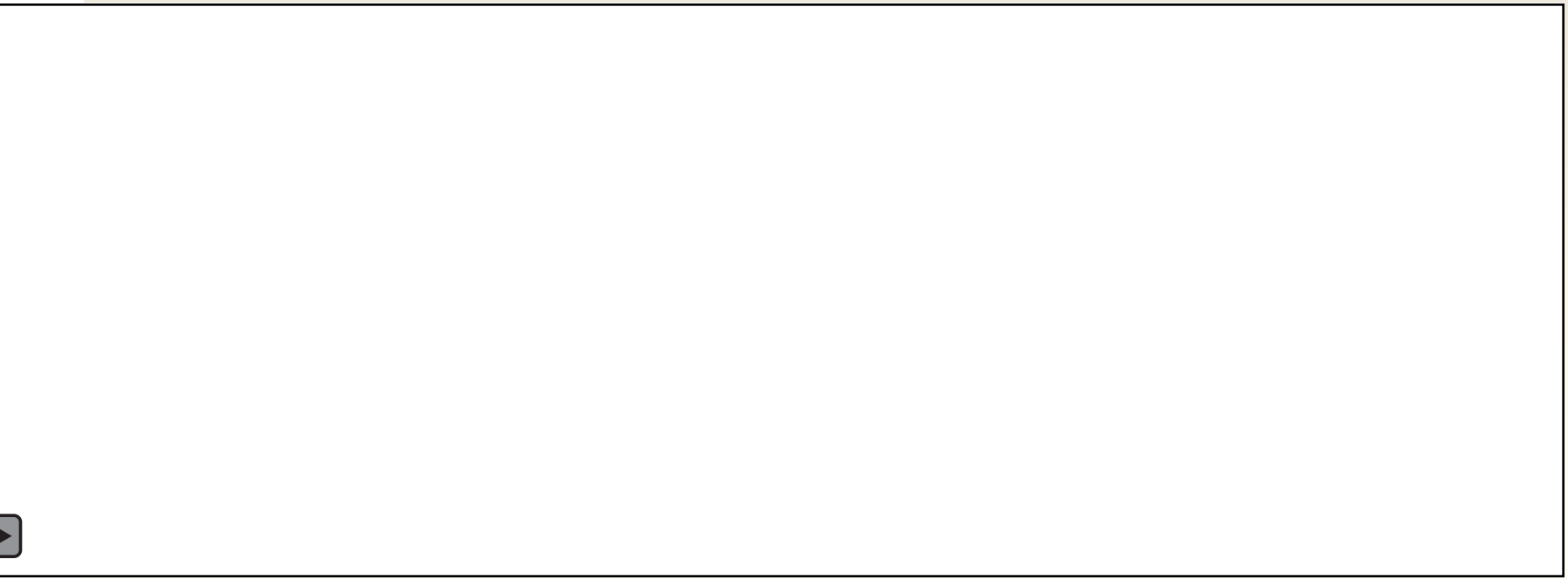
Two 3D EM Solvers – one problem, two answers, one big problem!



“What could possibly go wrong? - Retired engineer Ira Pollock, Tektronix

- Are you modeling what will be fabricated?
- Nominal or variation of impedance transmission lines may eat signal integrity (SI) margins
- Does the 3D EM EDA tool(s) actually work?
  - *“All tools have issues, it is up to the SI engineer to work around them”* – Scott McMorrow, CTO Samtec
- Will fabrication tolerances tank you by eating SI margin – is your material junk, is etching poor, how about lamination alignment for multi-lam?
- Loss Models and material ID fitted correctly, how accurate is laminate manufacturers data sheet?
- S-parameters and de-embedding quality ok?
- Stack-up suits 70GHz localization?
- Is the pcb system a resonant system within Fmax, fastest rise times?
- EM boundaries set right in solver?
- Meshing and Computational Tolerance set correctly?

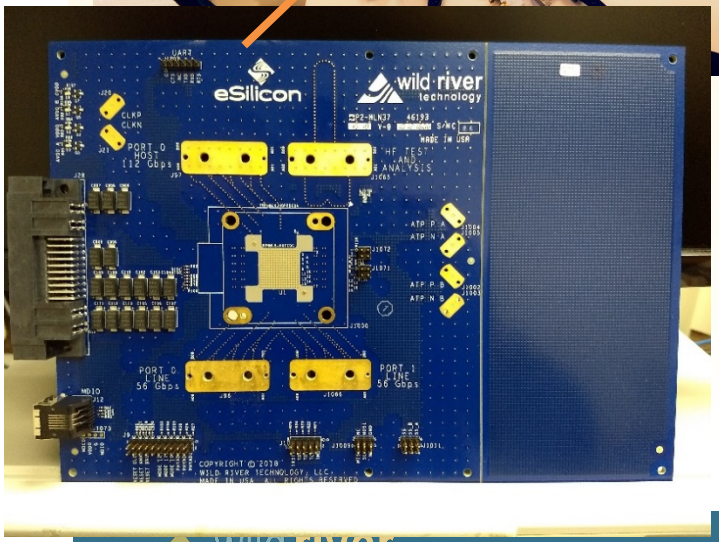
+50GHz Electromagnetic Optimization is Challenging



The Challenges of +50GHz SI

- **EDA Tools and Simulation Methodology**
  - **Benchmarking the tool**
  - **Methodology and Tuning Your Simulation**
- What Exactly is Good SI?
  - The answer is not always obvious!
  - IEEE P370 TG1
  - How many spins to get there?
- The “Alamo Strategy” for Test Fixture Architecture
  - The Tale of 2 Titanic Captains
  - Always have a way out, the “Alamo Strategy”
- The “Fabrication Hurdle” What is it, how to get past it
- New Paradigm for Critical SI Connector Vendor Working Relationships
- Why Program and Project Management gets in the way of 70GHz SI
  - Schedules versus Innovation and Building Technologies
  - Concurrent EDA Teams
- Closing Ideas
- Conclusion
- Open Discussion

The Challenge



- New 7nm eSilicon full DSP based 56Gbps SerDes IP (112G in fabrication)
  - Full access to SerDes lane monitoring capabilities
- **5m of Samtec cable, ExaMax** connectors, cabled backplane architecture
  - Smaller gauge than others, 40 pairs of 30 gauge 2mm bend radius twin-ax with only -4 dB of IL at 14 GHz Nyquist
- **Pre-FEC BER >4 orders of magnitude better than the IEEE 56G spec**
- New evaluation board targeting the **P370 IEEE specification** in draft
  - Beta version, production coming next month
  - **5 company collaboration**

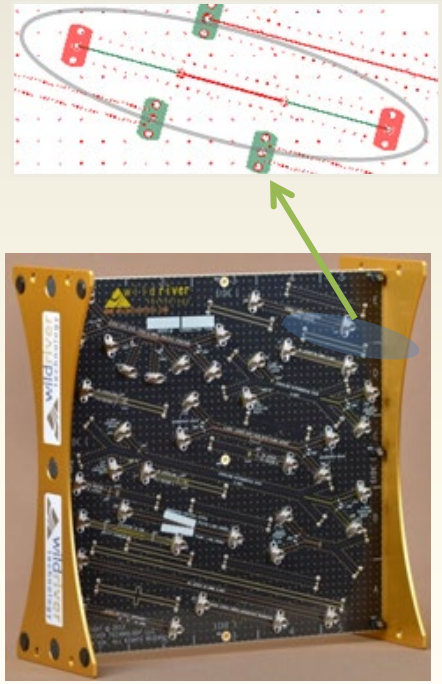
Particulars of This Platform

- 70GHz 112G PAM-4, stellar SI required
- Via fields (backdrilled, microvias)
- Multi-laminate construction
- Traces (mainly stripline, microstrip on ELF 1.85mm edge launch)
- ELF (edge) and vertical high-density launch like Samtec Bullseye(50, 70GHz) for all SERDES channels
- Complicated breakouts to a BGA
- Very complicated de-embedding

What is Objectives, Thoughts?

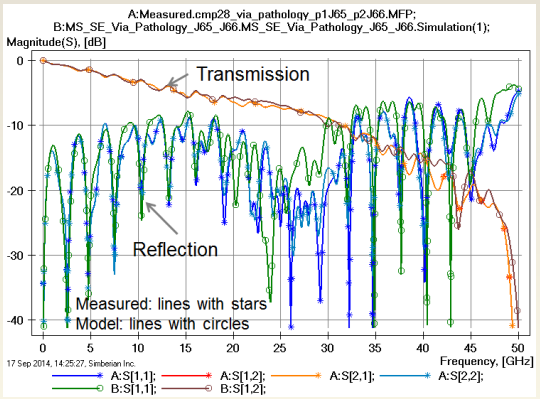
- **One fabrication spin**
- **Alamo Strategy** – always have a mitigation step for any risk element
- Several ways of doing one thing (example is de-embedding)
- **Team and Design Reduncancy**
- Continual Innovation to get there

Innovation - Benchmarking EDA Tool

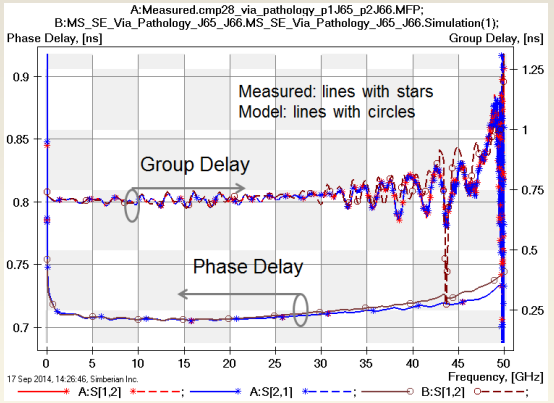


Example using Via-patho trace – Via, mimics connector and breakout field

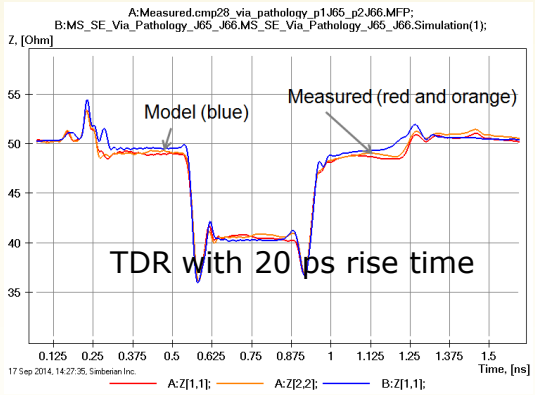
CMP-28 Channel Validation Platform from Wild River Technology LLC



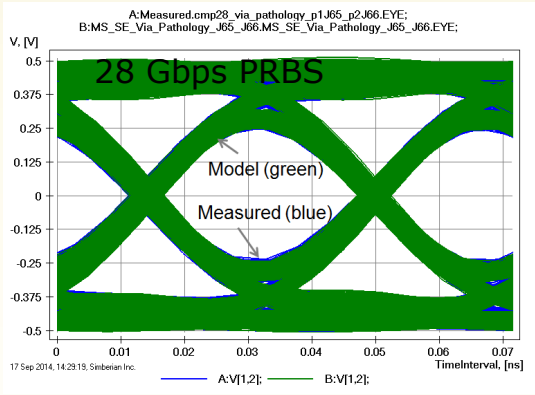
Frequency



Phase/Group Delay

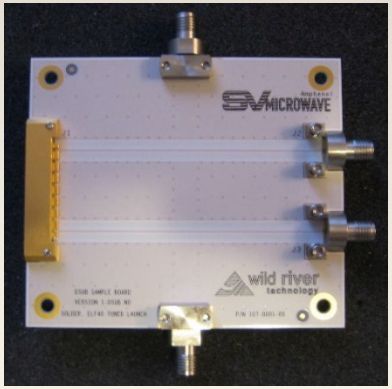


Time/TDR



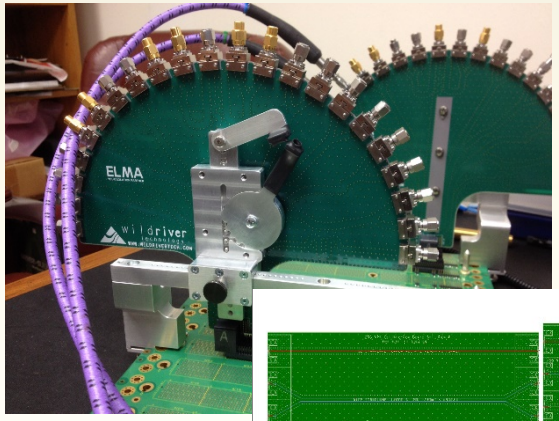
Time/Eye Diagram/Jitter

Example Benchmarking Test Vehicles

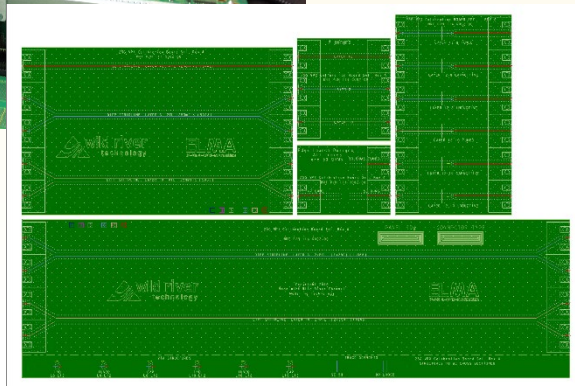


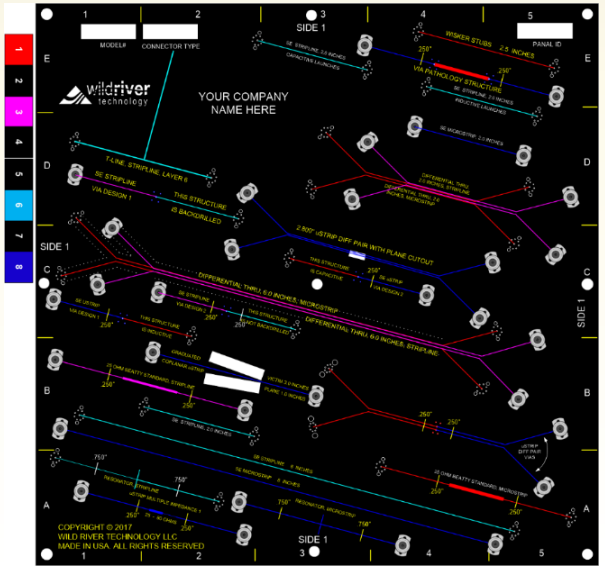
50GHz Test Fixture, Soldered connector

50GHz Test Channel Modeling Platform



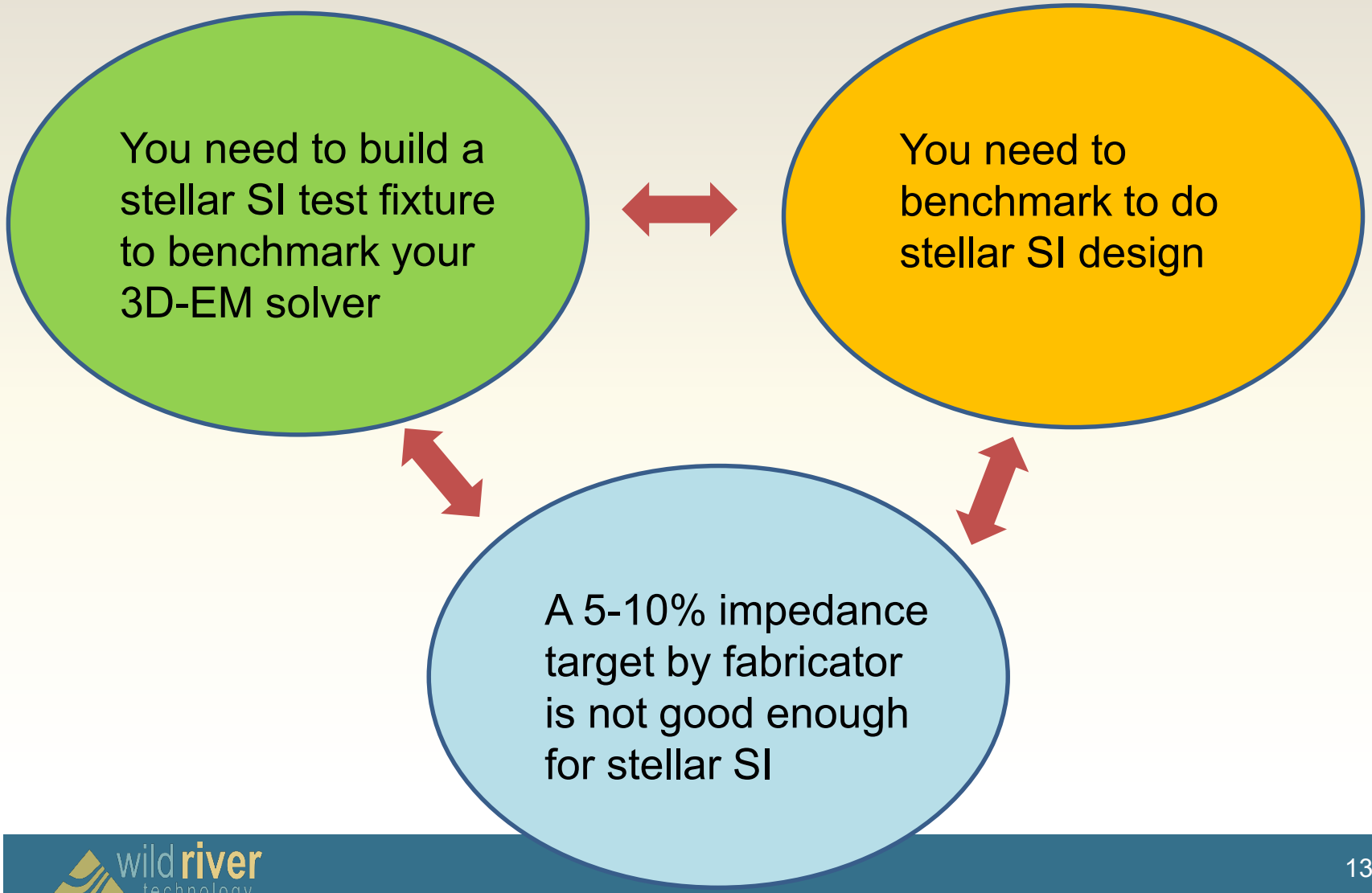
25G Test Fixture and companion CMP for backplane analysis





For material identification and laminate demonstration

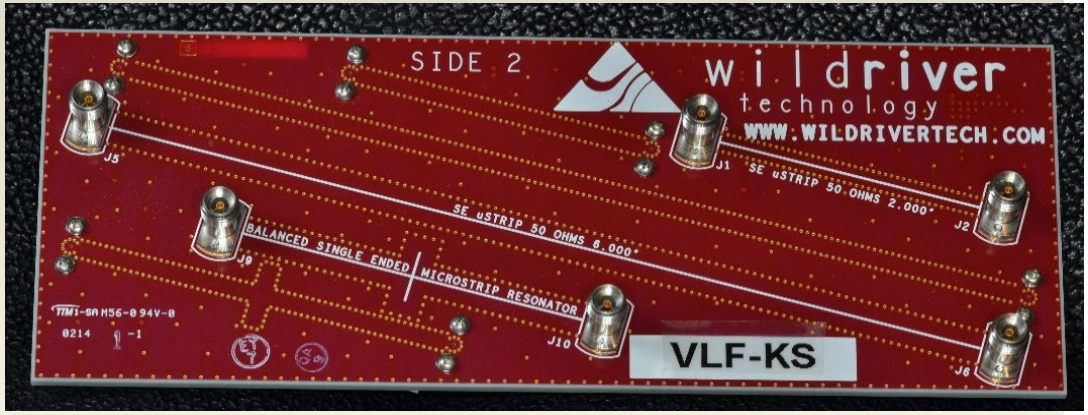
The Benchmarking Conundrum



Assuming +50GHz Benchmarking Test Fixtures are difficult to design, How Can you Make Things Simpler/Easier?

Solution to Conundrum: **Blitzkrieg Signal Integrity**

"A good answer now is often better than a better answer later" - Eric Bogatin inspired



CMP-MiniX, not showing cross section analysis

- Validate stackup and fabrication
- Launch Design
- Material Homogeneity, Etch Variation
- Cross section analysis
- Loss Modeling (surface roughness lumped into conductive loss at this stage), Material Modeling – HFSS, Simbeor
- Launch Design Validation

Your not ready for *The Challenge* if you don't have a

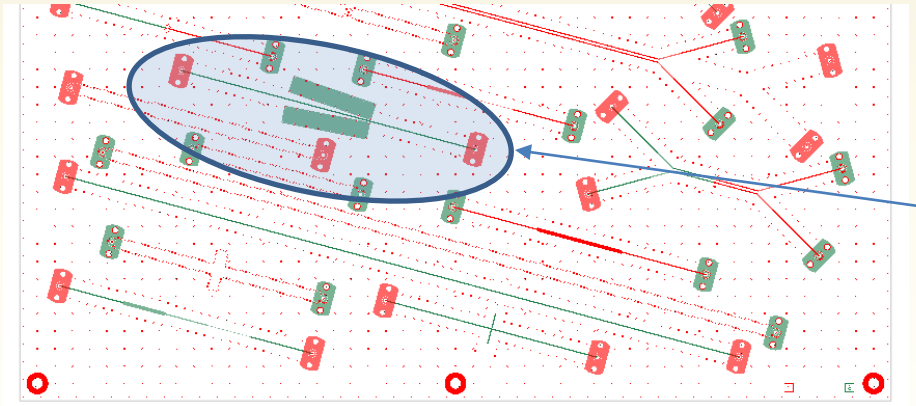
1. **Clear methodology** based on ongoing innovation
2. **Benchmarking** – know your 3D EM EDA tool
3. **Identified critical crux elements**, have mitigation strategies for each

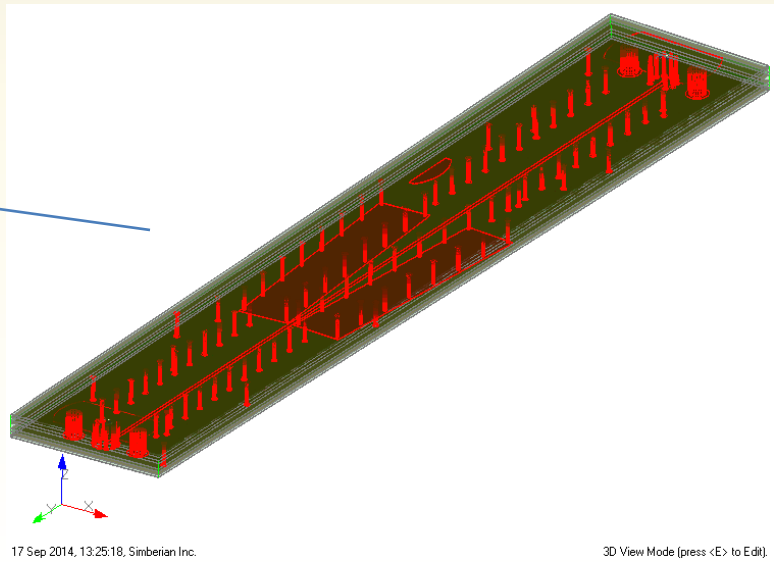
What Do You Need for Benchmarking?

- For material ID and loss model development
- For **loss model verification**
- **3D EM analysis specific** (will see example)
- **Specific to system** (connectors, BGA breakouts)
- **Cross section structures** for determining what was fabricated

Example of a 3DEM Specific Benchmarking Structure

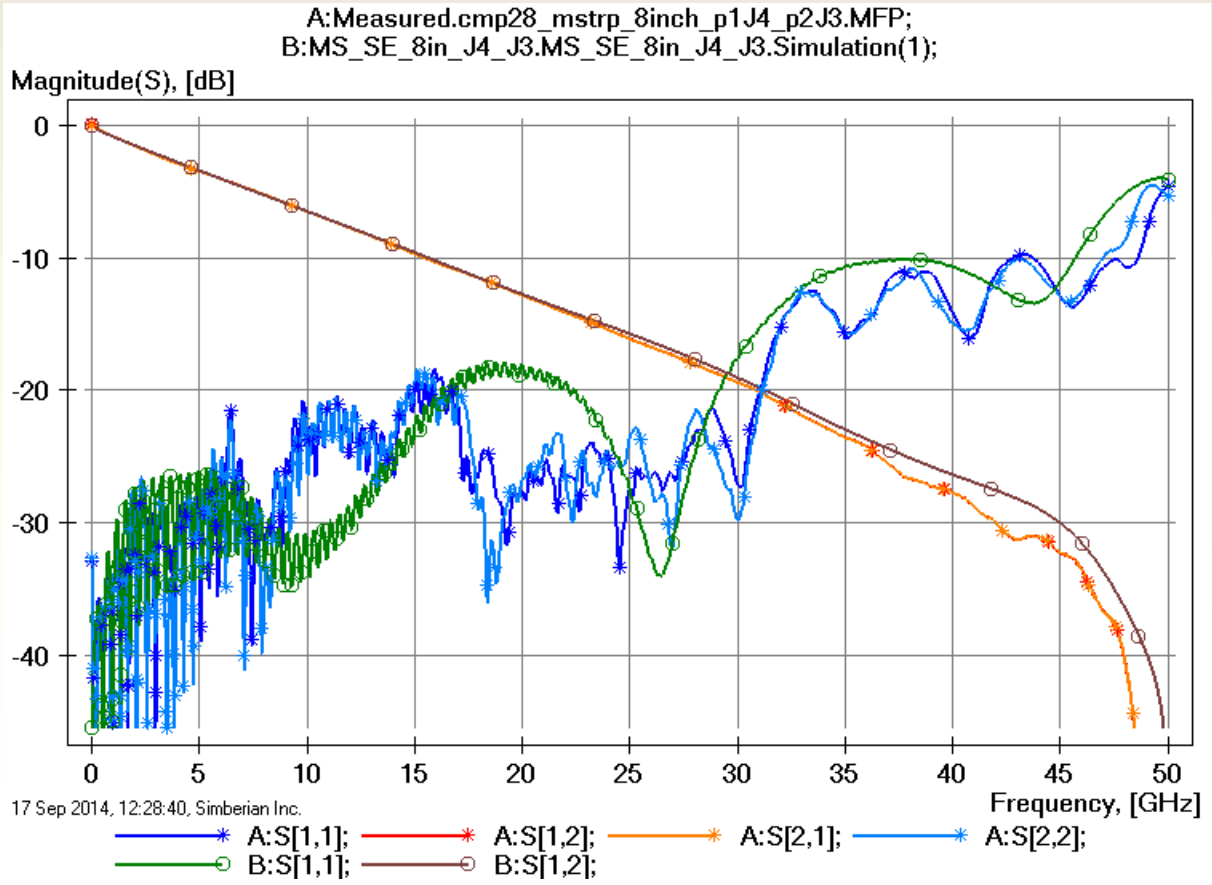
- Always have benchmarking objectives and associated priority
- Many structures have multiple roles, some only have one





Graduated coplanar structure has one purpose: Benchmark meshing in 3D EM solver

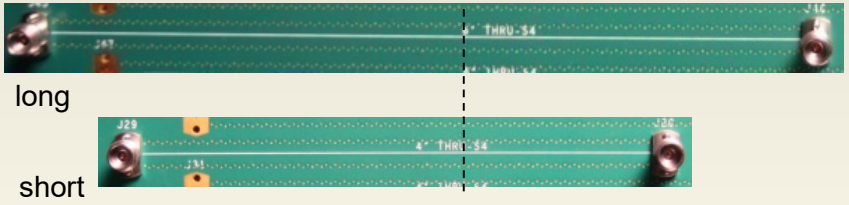
Low-Loss and Low Reflection does not Benchmark return-loss very well (S11, S22, SDD11), **Essential for SDD21 or S21 However**



8inch microstrip line example, difficult to match S11, S22 due to impedance/fabrication issues

Note 50GHz measurement BW but 2.92mm 40GHz connectors are used – discussed later.

Always Start with 2 T-lines, 2 Lengths as the most basic **Primitive**: Scores of applications – Loss modeling, de-embedding, fabrication verification, launch analysis



2 Line segments, a short one and a long one

Cross-section analysis is required for 28-112G level work, essential to determine as-fabricated

2 Transmission lines and a cross sectional analysis provides reams of useful SI information and analysis

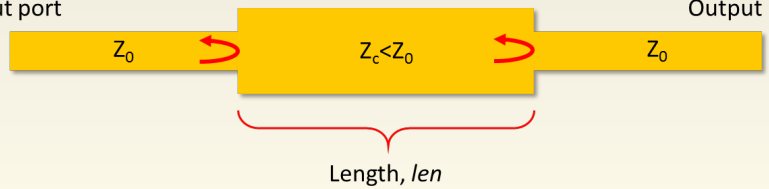
Resonators – example of Beatty Standard, very useful structure

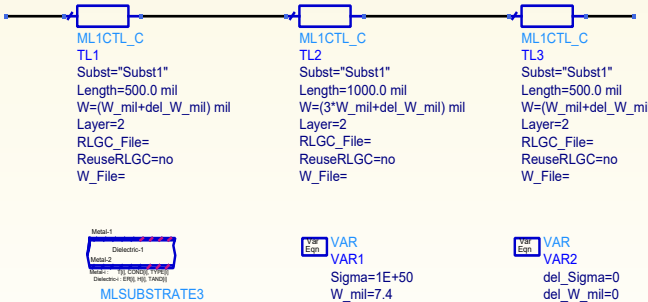
Port 1
Input port

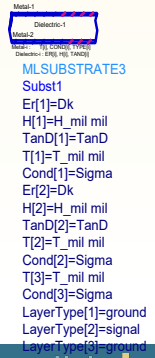
$\Gamma_{front} < 0$

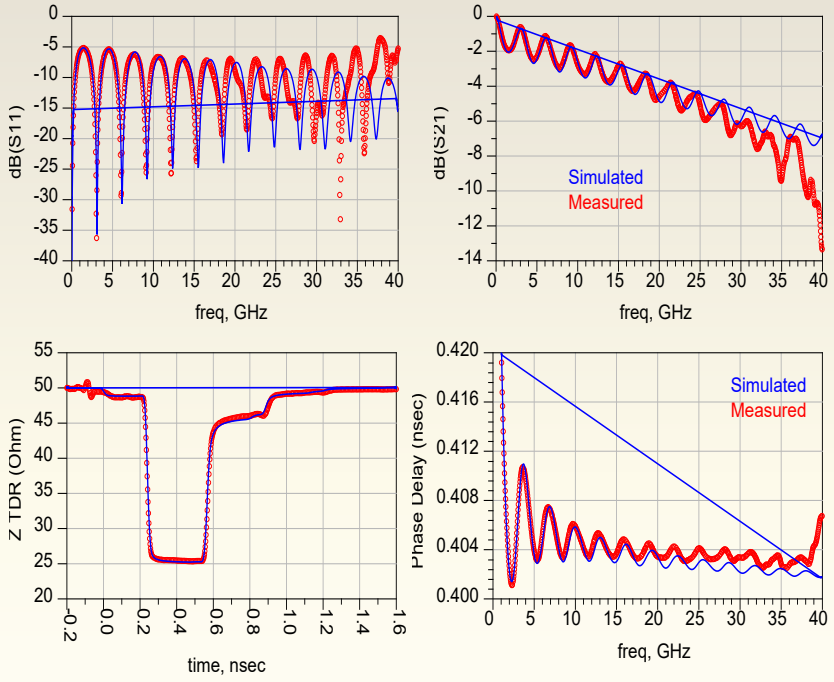
$\Gamma_{back} > 0$

Port 2
Output port







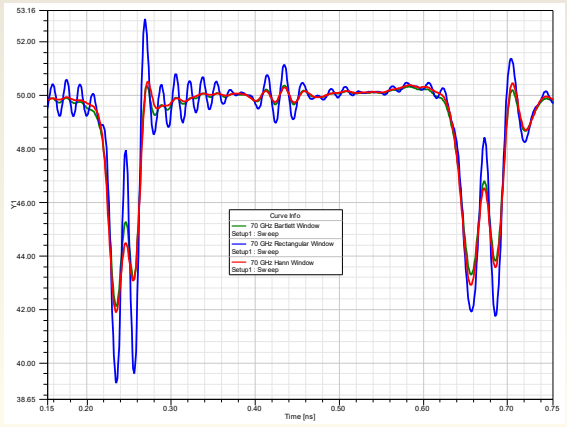


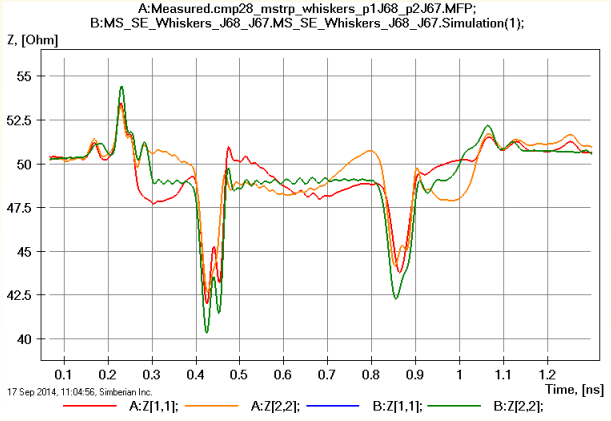
Matching simulation to measurement using Beatty Standard

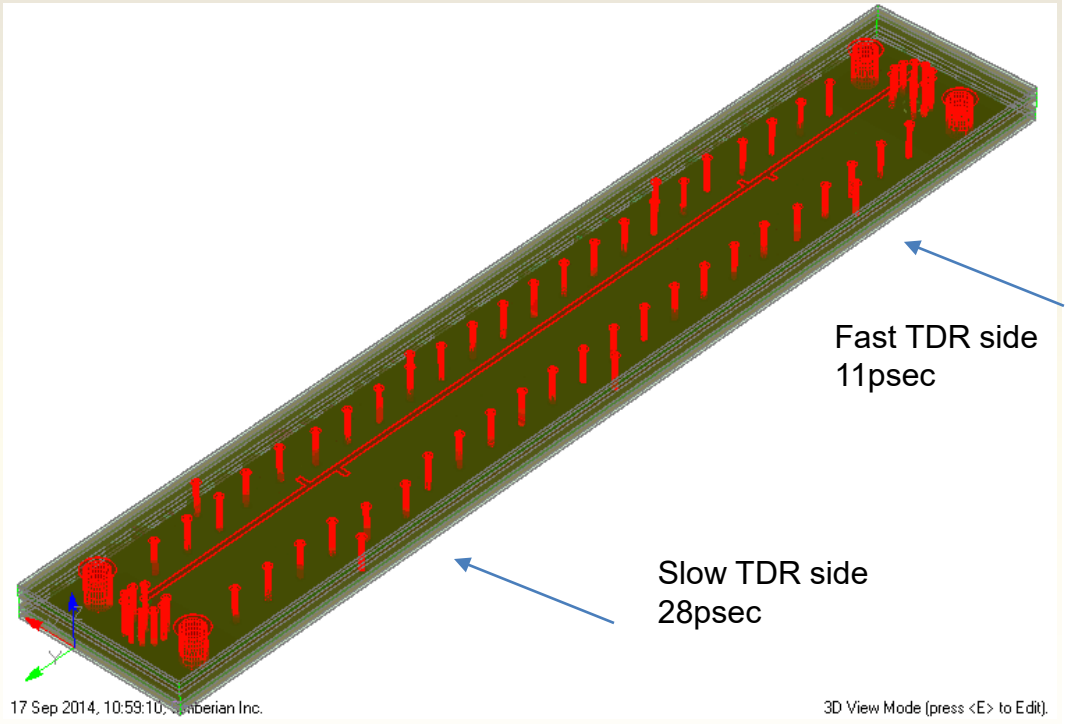
EDA analysis of this standard is straightforward by careful de-embedding is required

Time Domain versus Frequency Domain is difficult – use both VNA and TDR

Unite Time domain TDR, VNA S-parameters, and 3DEM Solver analysis



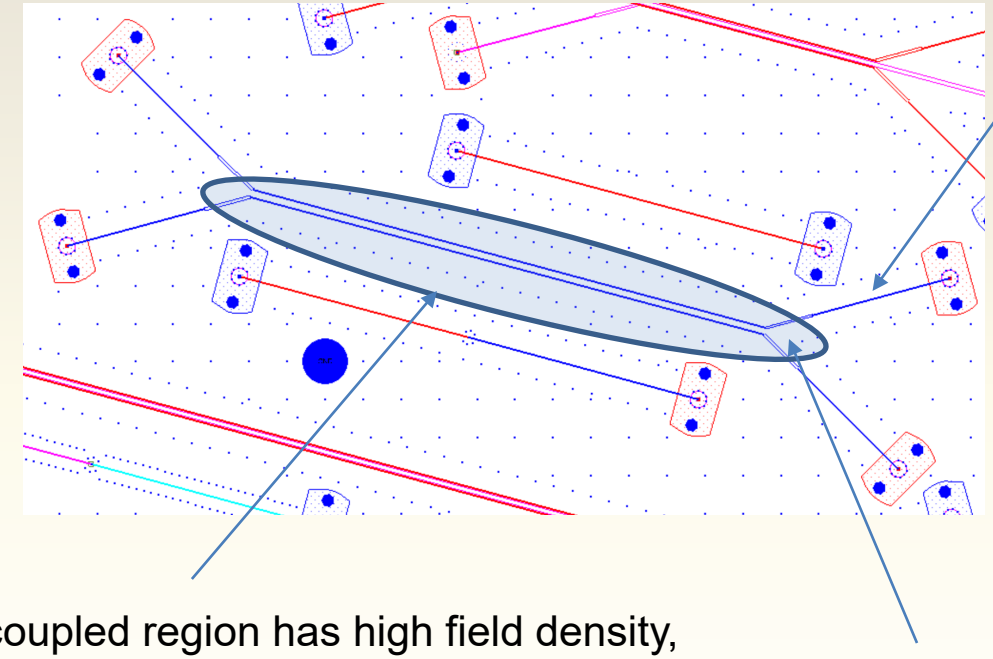




Time domain whisker stubs for fast/slower TDR, upper left is TDR, lower left is VNA data to EDA

From DesignCon2014" Cracking the Code of 32Gbpsec Differential VIA's with Advanced Time Domain Methods"

Differential benchmarking, SDD21, SCD21, acts as 2X DIFF THRU, **Primitive** for DIFF circuits



SE region

The coupled region has high field density, important to use cross sectional analysis geometries and material ID for

SE to DIFF region benchmarking

Good Read: **Cracking the Code of 32Gbpsec Differential VIA's with Advanced Time Domain Methods**, DesignCon2014 Josiah Bartlett, Tektronix, Inc, Michael Steinberger, SiSoft, Inc., Alfred Neves, Wild River Technology LLC

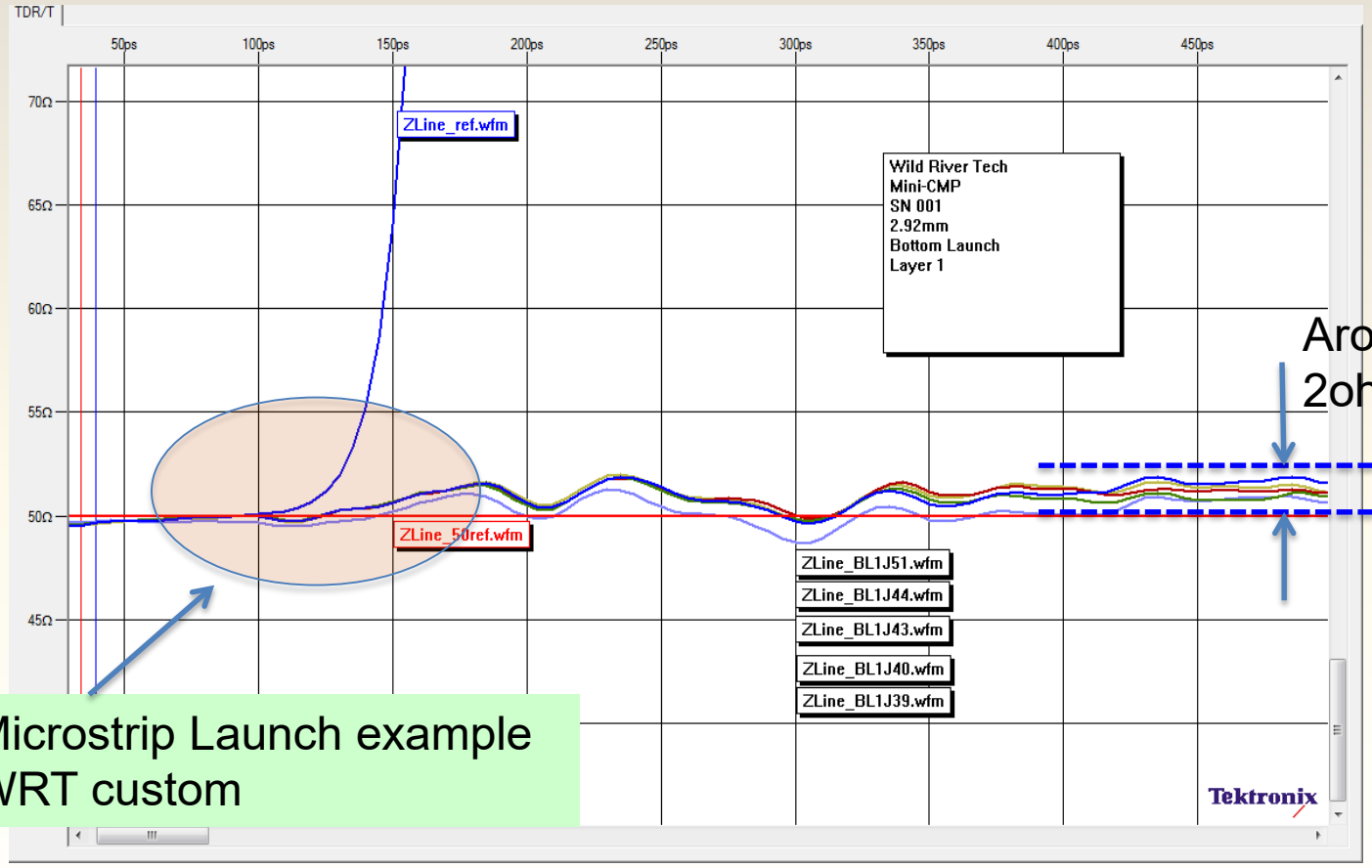
Benchmarking Limitations

- Your benchmarking confidence over a bandwidth is completely constrained by the test fixture signal integrity over that bandwidth
- **Junk test fixtures provide ability to do only junk engineering, *junk-begets-junk***

The Challenges of +50GHz SI

- EDA Tools and Simulation Methodology
  - Benchmarking the tool
  - Methodology and Tuning Your Simulation
- **What Exactly is Good SI?**
  - **The answer is not always obvious!**
  - **IEEE P370 TG1**
  - **How many spins to get there?**
- The “Alamo Strategy” for Test Fixture Architecture
  - The Tale of 2 Titanic Captains
  - Always have a way out, the “Alamo Strategy”
- The “Fabrication Hurdle” What is it, how to get past it
- Why Program and Project Management gets in the way of 70GHz SI
  - Schedules versus Innovation and Building Technologies
  - Concurrent EDA Teams
- Closing Ideas
- Conclusion
- Open Discussion

Example of a 2 Ohm System using 7psec Tek TDR

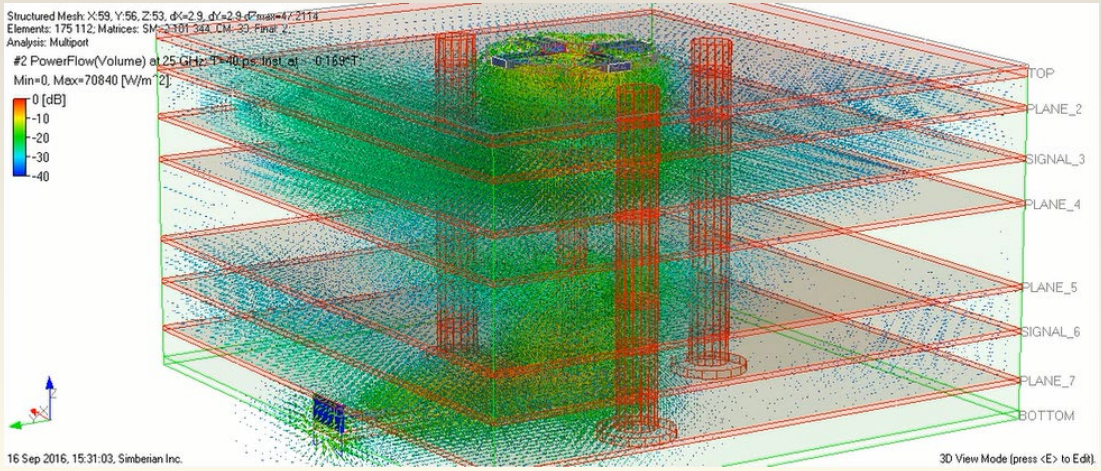


Around 2ohms

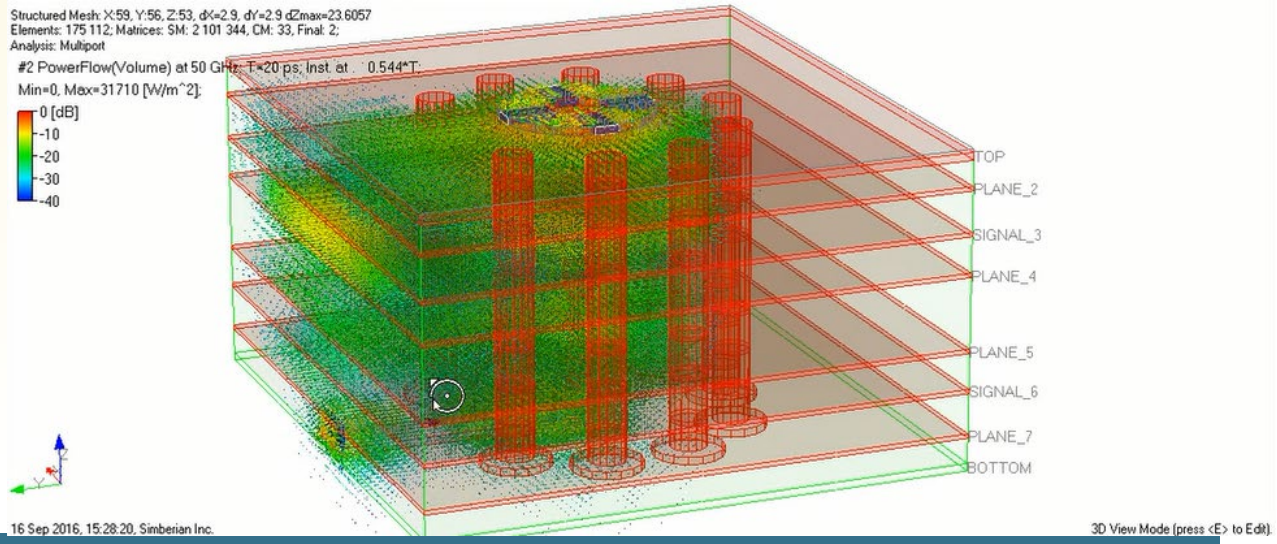
Microstrip Launch example
WRT custom

Localization or Energy Leaking out of System – IEEE P370 calls for 30mils separation – Subtle SI Issue!

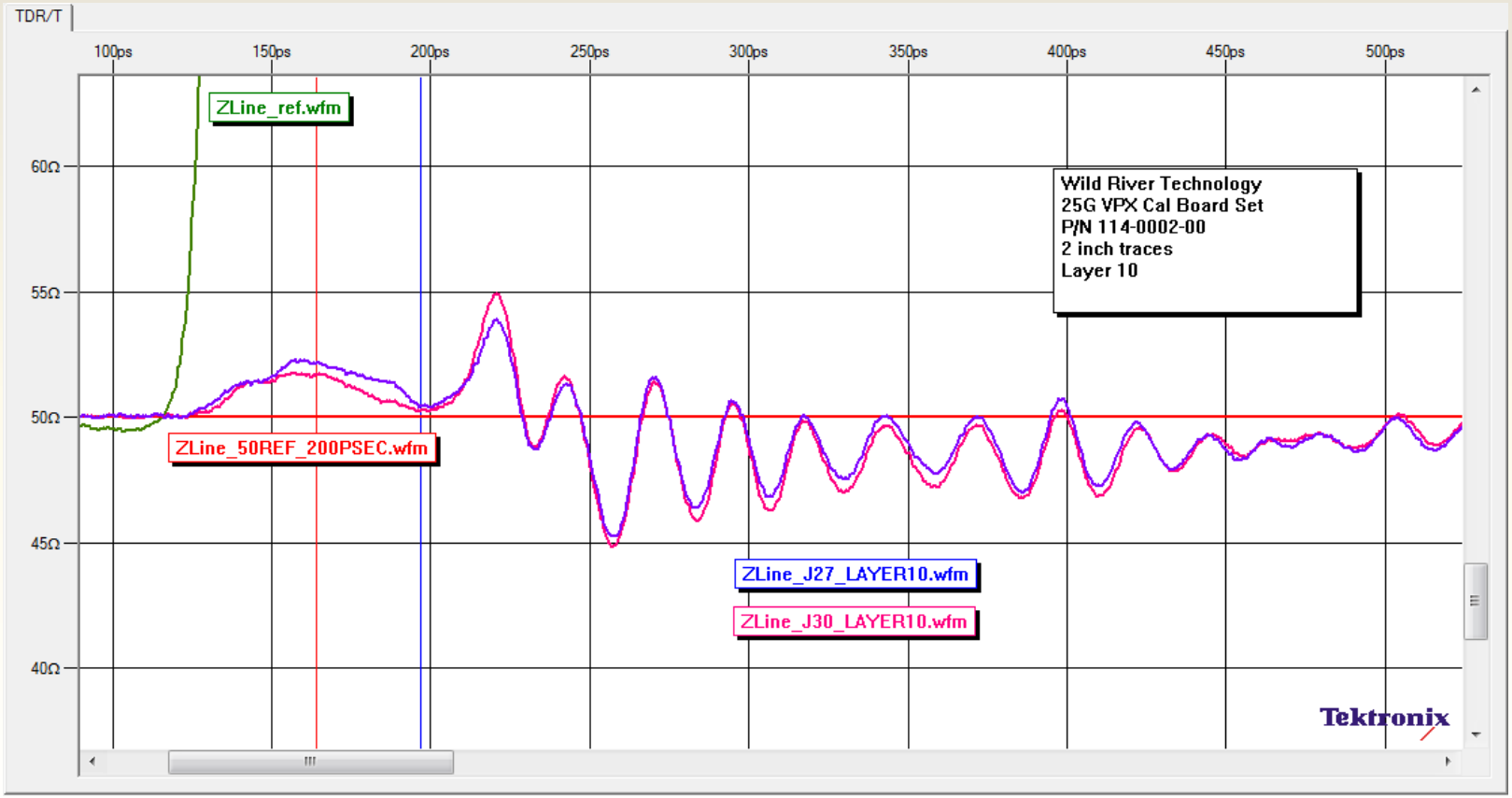
25GHz with only 3 vias – poor localization but moderate high frequency shows localization issues, power spreading to planes outside structure



50GHz with moderately high localization using 9vias, power flow starts to escape structure



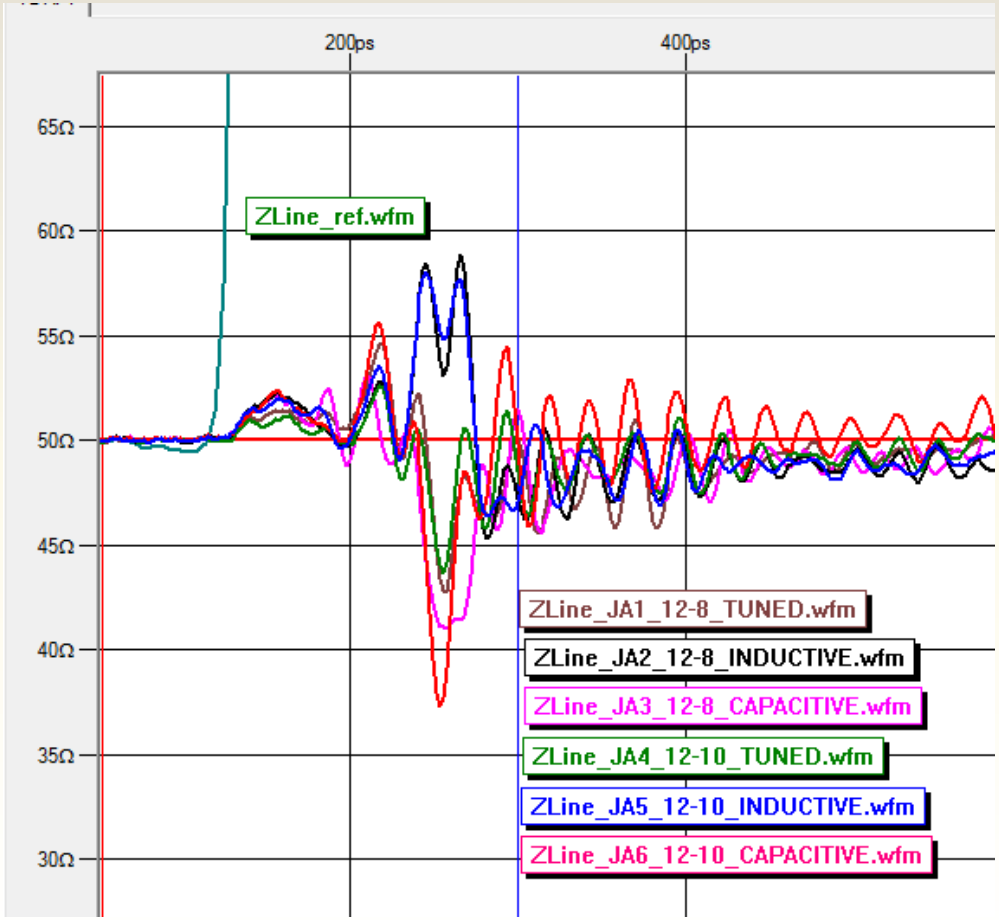
Stackups are Subtle – We see a lot of resonant systems



Breaking things helps you to fix things later and achieves improved 3D EM benchmarking

Broken structures become valid test structures as well!

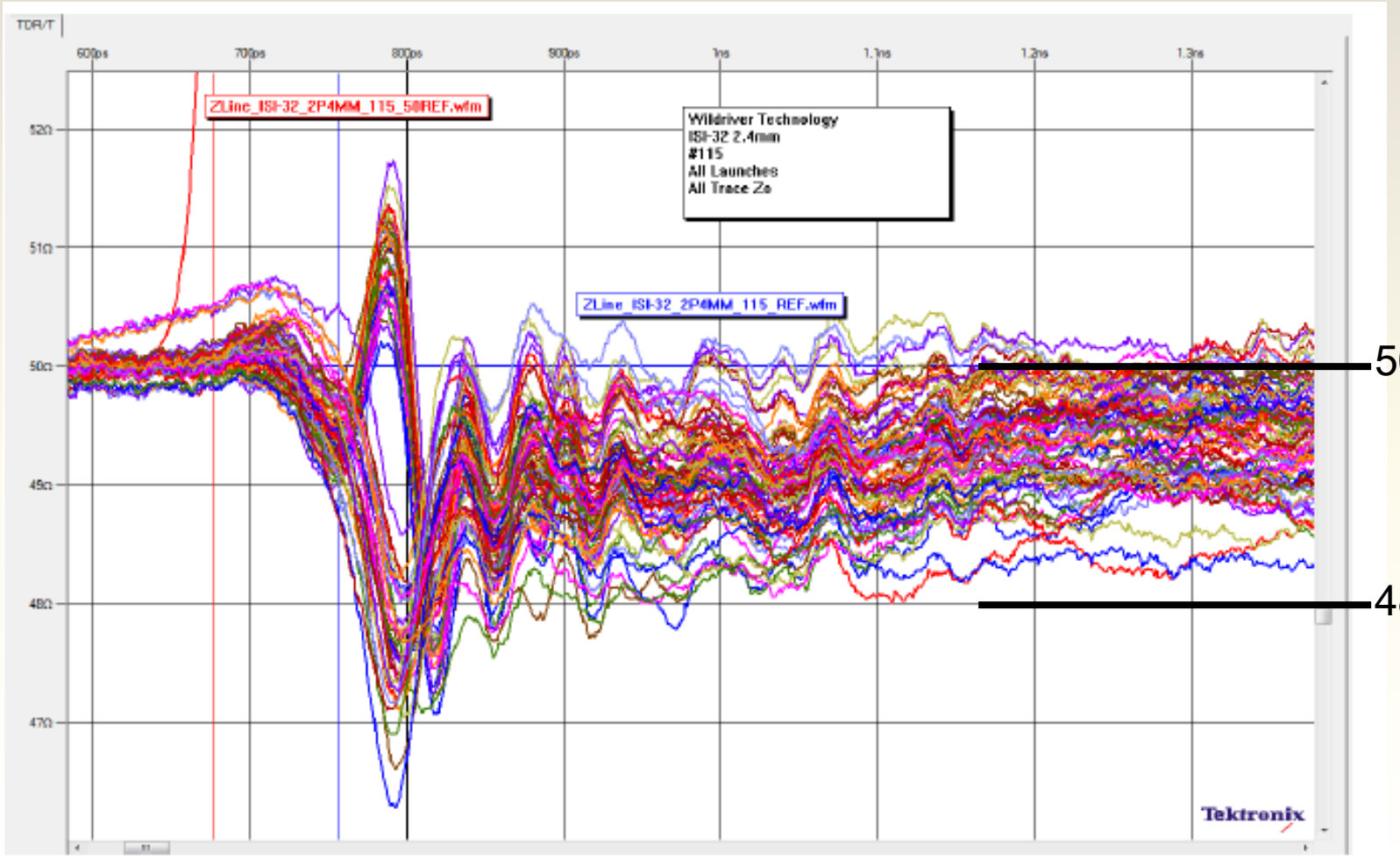
Breaking Things is Good
New concept: ***Intra-DUT***



55ohms

45ohms

Variation across Test Fixture – Launch Integrity, material homogeneity, *TDR EVERYTHING!*



ZLine of all launches and traces

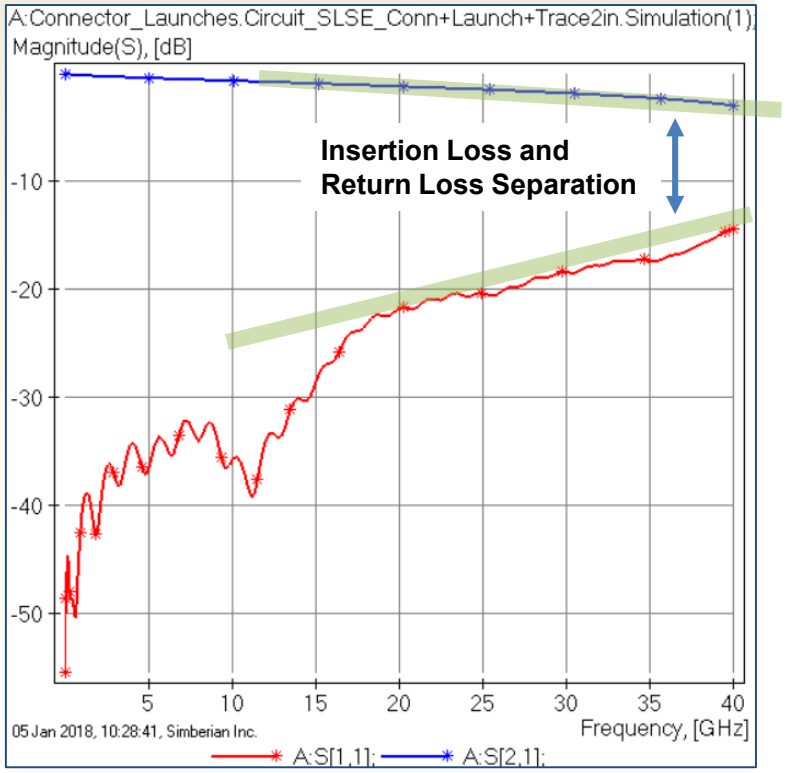
IEEE PG370 Emerging Standard

- **Test fixture**
  - Definitions and common language, metrics, topology
- **S-parameter Quality**
  - Causality, passivity, VNA set up, calibration verification
- **De-embedding**
  - Quality, approach, tools to veriy

Example TG1, Test fixture metrics

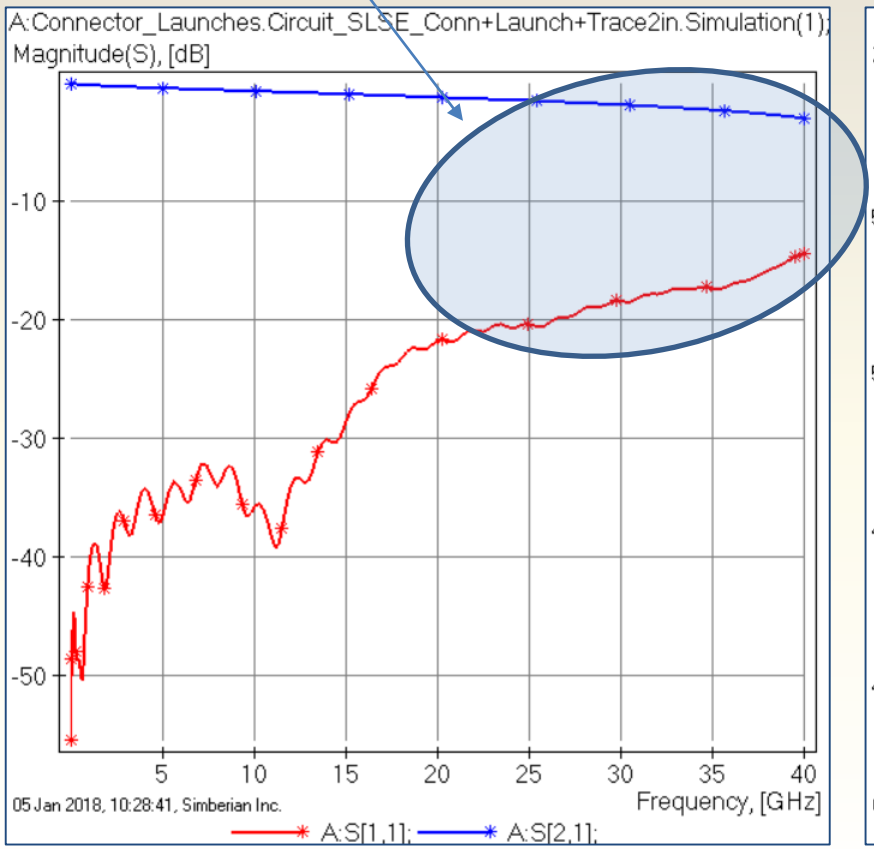
FER3: Insertion Loss and Return Loss Separation

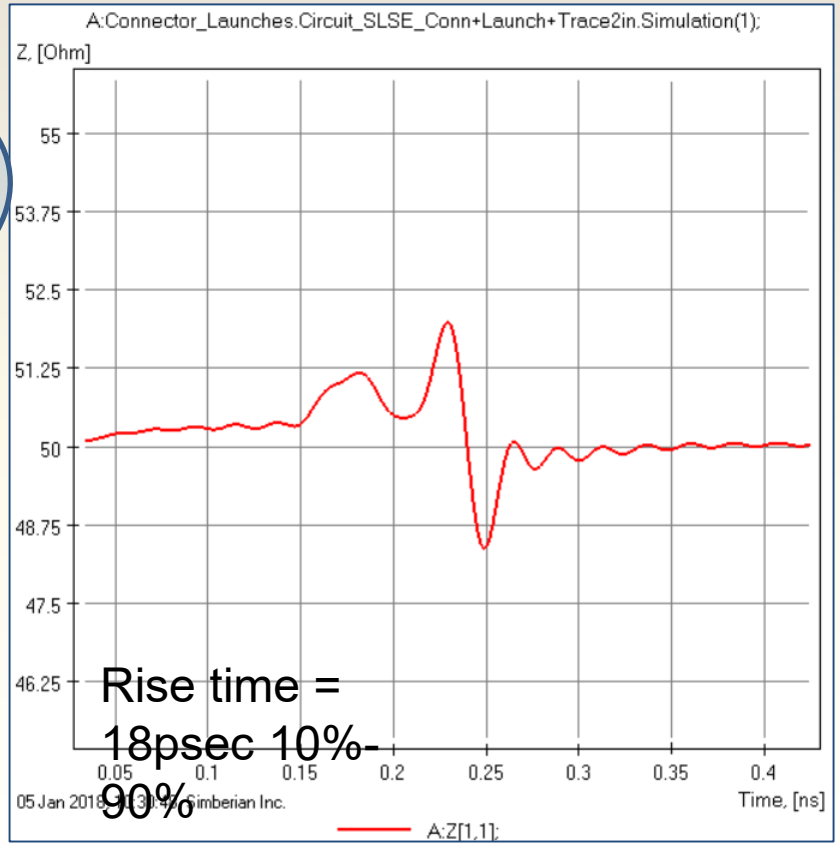
- Class A Maximum: 5 dB at all frequencies of interest
- Class B Maximum: 0 dB at all frequencies of interest.
- Class C Maximum: 0 dB at all frequencies of interest



Stripline Tuned Launch Design – meets top IEEE PG370 metric

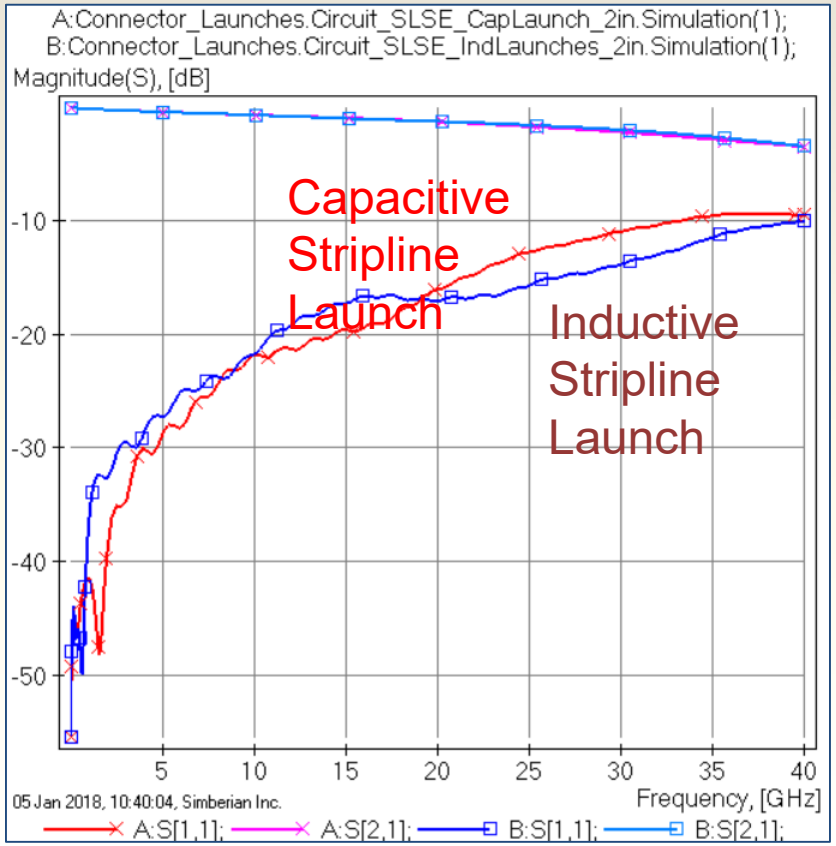
Very good S21/S11 margin

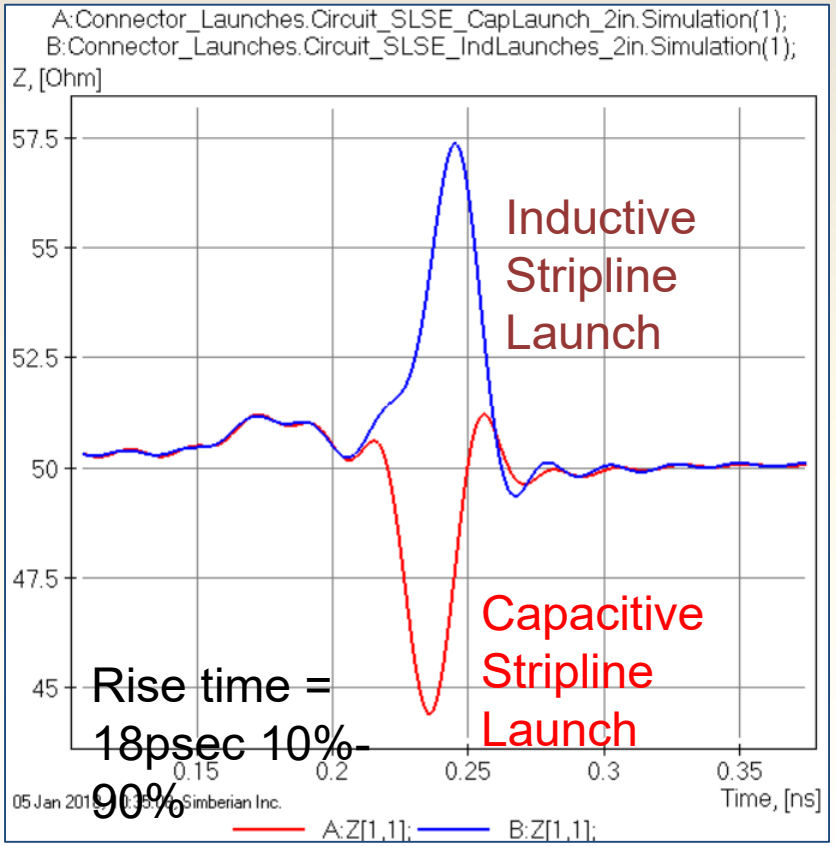




Rise time = 18psec 10%-90%

Stripline Untuned Launch Designs





HD Very High-Speed Interconnects – What Should You Expect from Vendor – ***Stop Coddling Vendors!***

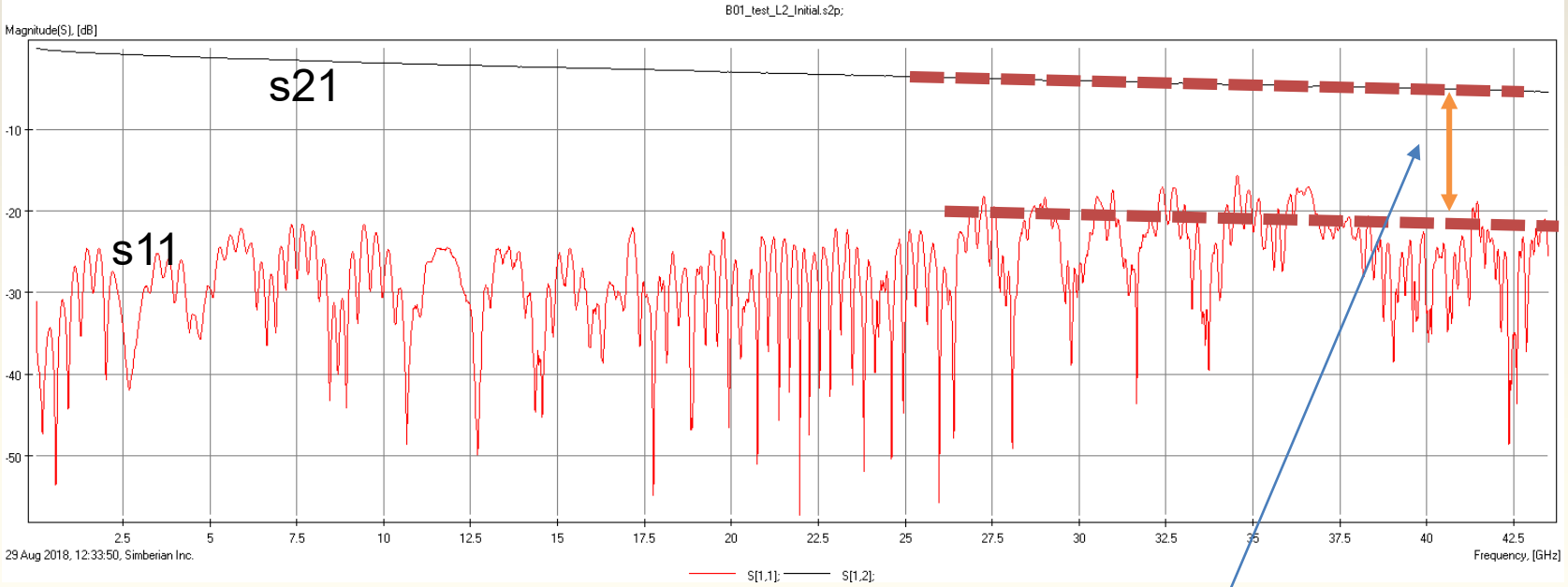
1. What electrical characterization was done by your team? Then use IEEE P370 metrics to evaluate SI.
2. Is that fixture available for us to borrow?
3. What time domain gating was done or fancy post processing to evaluate connector?
4. What is connector repeatability channel-to-channel with TDR overlay, skew.
5. What is quality of the total interconnect using fast TDR (2psec) from coaxial 1.85male connector- cable-HD interconnect.
6. If you twist the connector cable 90degrees off axis does the S-parameters change (SMP connectors have a big problem with this). This performance is critical.
7. How good is their 3D EM optimization support, reports, step and dxf file support? Start with a return loss mask that has a clear S11 goal.
8. What is their model quality? Not convinced an encrypted HFSS model of actual connector is the right model for these demanding SI apps.
9. Measure TDR of scores of channels and overlay impedance profiles for all the measurements
10. How good is the mechanical interconnector, bulkhead housing and associated integrity.

Samtec, Bullseye 70GHz

S-parameter Work Flow: Quality was good

File name	Quality	Passivity	Reciprocity	Causality
E:\WRT_Bullseye2__28_18				
A05_test_L3_Initial.s2p	-	100	98.6	75
B01_test_L2_Initial.s2p	-	100	98.4	77.6
B01_test_L2_TB.s2p	-	100	98.8	77.6
B01_test_L2_TL.s2p	-	100	98.5	77.8
B01_test_L2_TR.s2p	-	100	98.7	77.8
B01_test_L2_TT.s2p	-	100	98.8	80.1
B03_test_L3_Initial.s2p	-	100	98.9	79.1
B03_test_L3_TB.s2p	-	100	98	79.4
B03_test_L3_TL.s2p	-	100	98.9	79.6
B03_test_L3_TR.s2p	-	100	97.4	78.7
B03_test_L3_TT.s2p	-	100	99	81.2
B05_test_L4_Initial.s2p	-	100	98.8	78.3
B05_test_L4_TB.s2p	-	100	99.1	78.9
B05_test_L4_TL.s2p	-	100	98.8	79.3
B05_test_L4_TR.s2p	-	100	98.5	79.2
B05_test_L4_TT.s2p	-	100	99	80.3
B06_test_L4_Initial.s2p	-	100	99	76.8
B07_test_L2_Initial.s2p	-	100	98.9	77
B10_test_L3_Initial.s2p	-	100	98.7	76.9
calTHRU.s4p	-	100	99.2	48.4

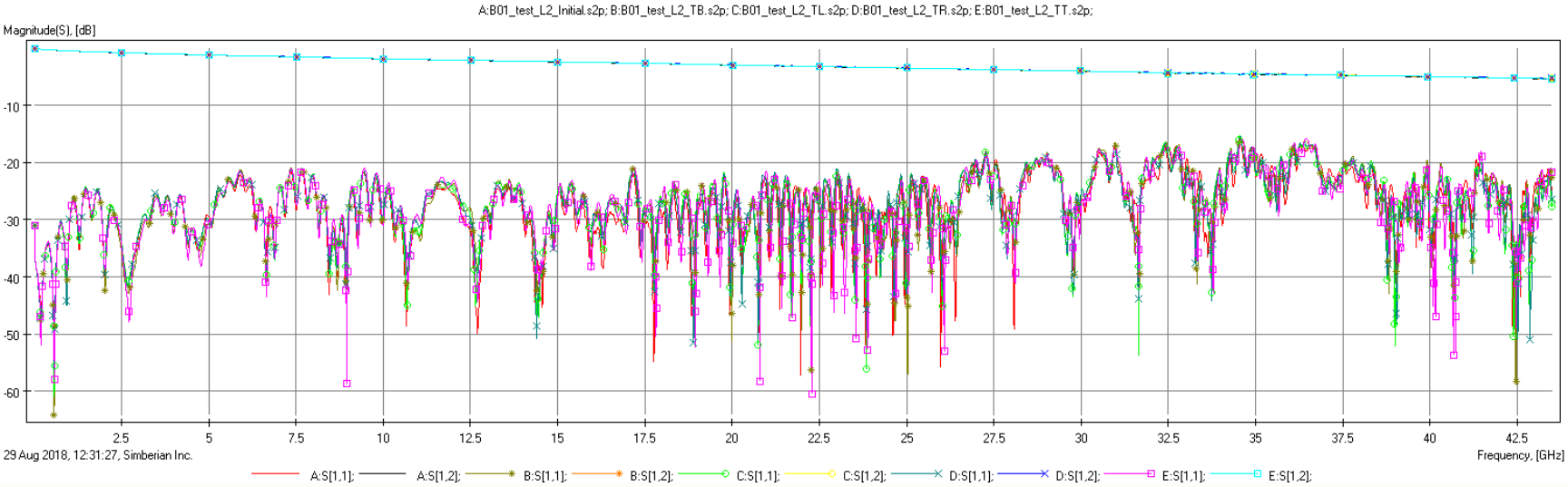
Signal Integrity, B01 channel, Layer 2 stripline



- Signal integrity is good past 43GHz
- No nasty resonance issues due to small launch pad, good connector SI, and good 3DEM optimization, and think layer

The closure between red dashed lines shows excellent signal integrity, with approx. 15dB margin.
This is insertion loss versus return loss margin and is detailed in IEEE PG370 specification for test fixture quality

We bent the coaxial cable breakout 90degrees left, right, up, and down, and included straight up as initial, very low variation as evidence in S-parameter overlay of all the measurements

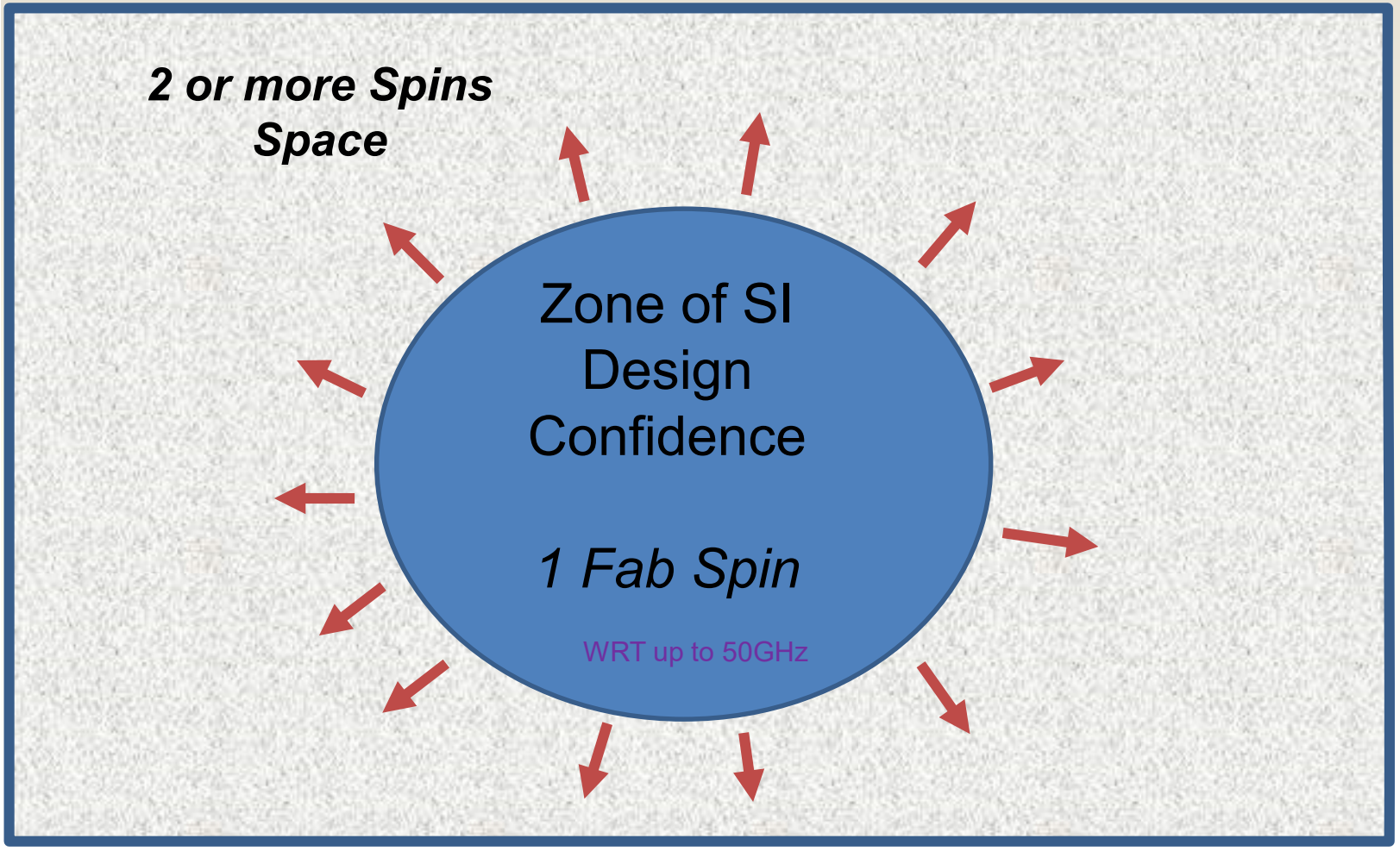


What can possibly go wrong? Go back a few slides to connector

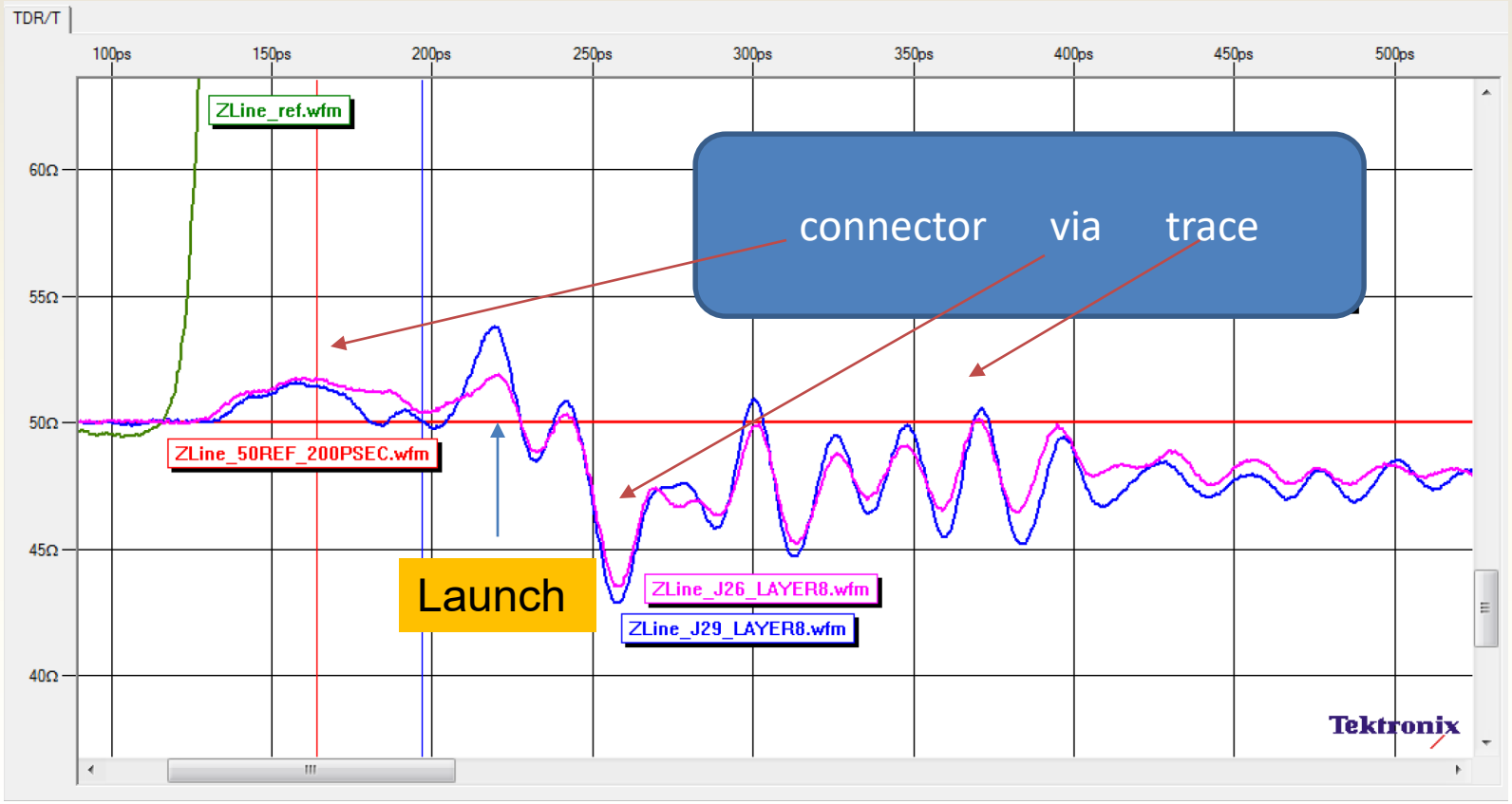
The Challenges of +50GHz SI

- EDA Tools and Simulation Methodology
  - Benchmarking the tool
  - Methodology and Tuning Your Simulation
- What Exactly is Good SI?
  - IEEE P370 TG1
  - Test Fixture Example?
- **The "Alamo Strategy" for Test Fixture Architecture**
  - **Zone of SI Confidence**
  - **The Tale of 2 Titanic Captains**
  - **Always have a way out, the "Alamo Strategy"**
- The "Fabrication Hurdle" What is it, how to get past it
- Why Program and Project Management gets in the way of +50GHz SI
  - Schedules versus Innovation and Building Technologies
  - Concurrent EDA Teams
- Closing Ideas
- Conclusion
- Open Discussion

Building Technologies and Innovating – Make Zone Confidence Bigger



Let's analyze SI and Discuss – Edge launch into Stripline, Think 32Gbpsec

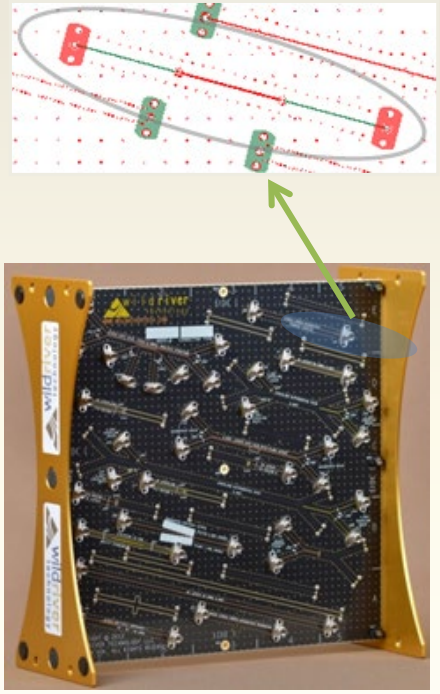


Future Projects – This Speaks to Project Management

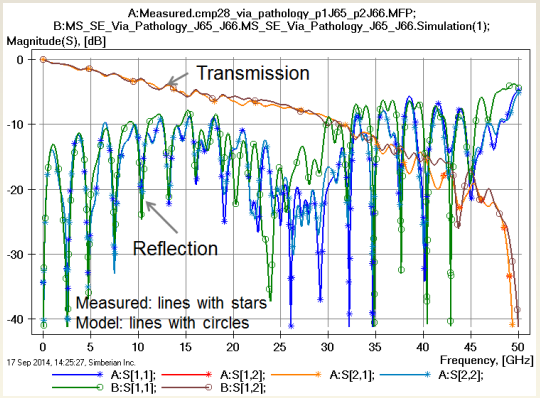
- Identify all Crux Technologies
- Determine if those design methodologies are in your Zone of Design Confidence
- What innovations and technologies need to be developed

Channel Modeling Methodology

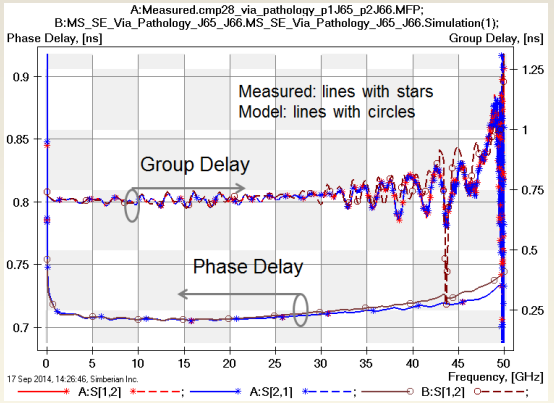
Testing Design Zone of Confidence



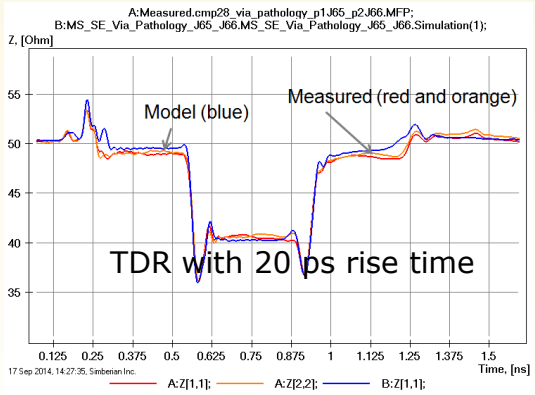
CMP-32 Channel Validation Platform from Wild River Technology LLC, example of structure that mimics connector



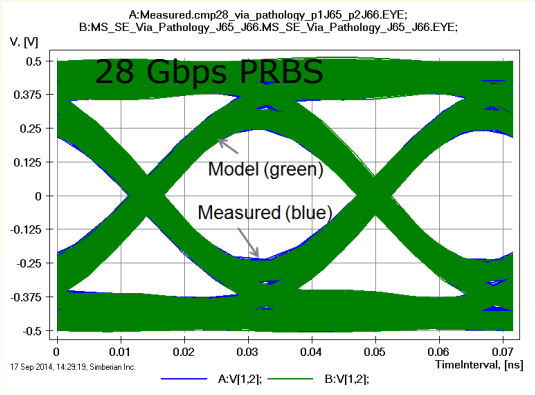
Frequency



Phase/Group Delay

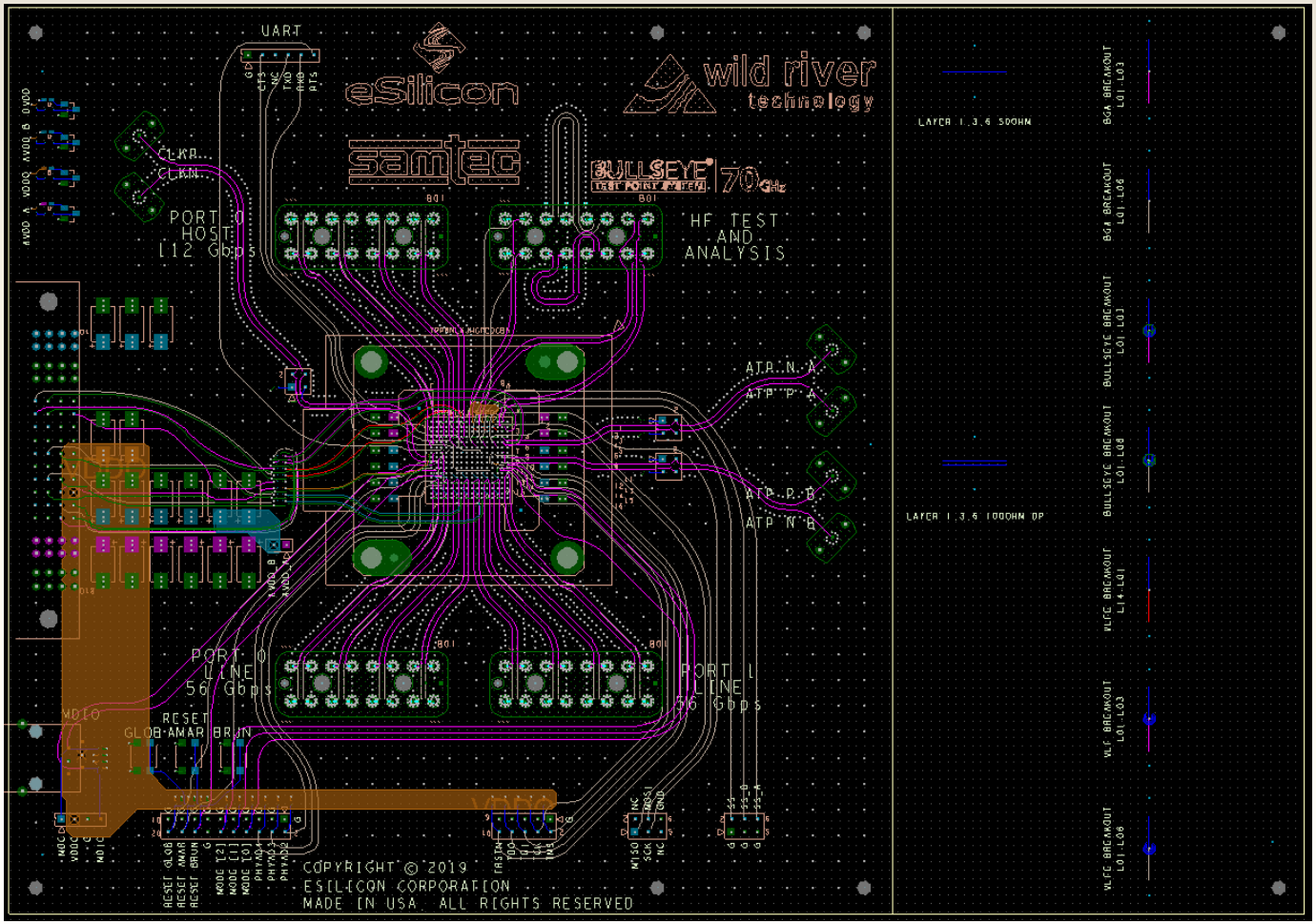


Time/TDR

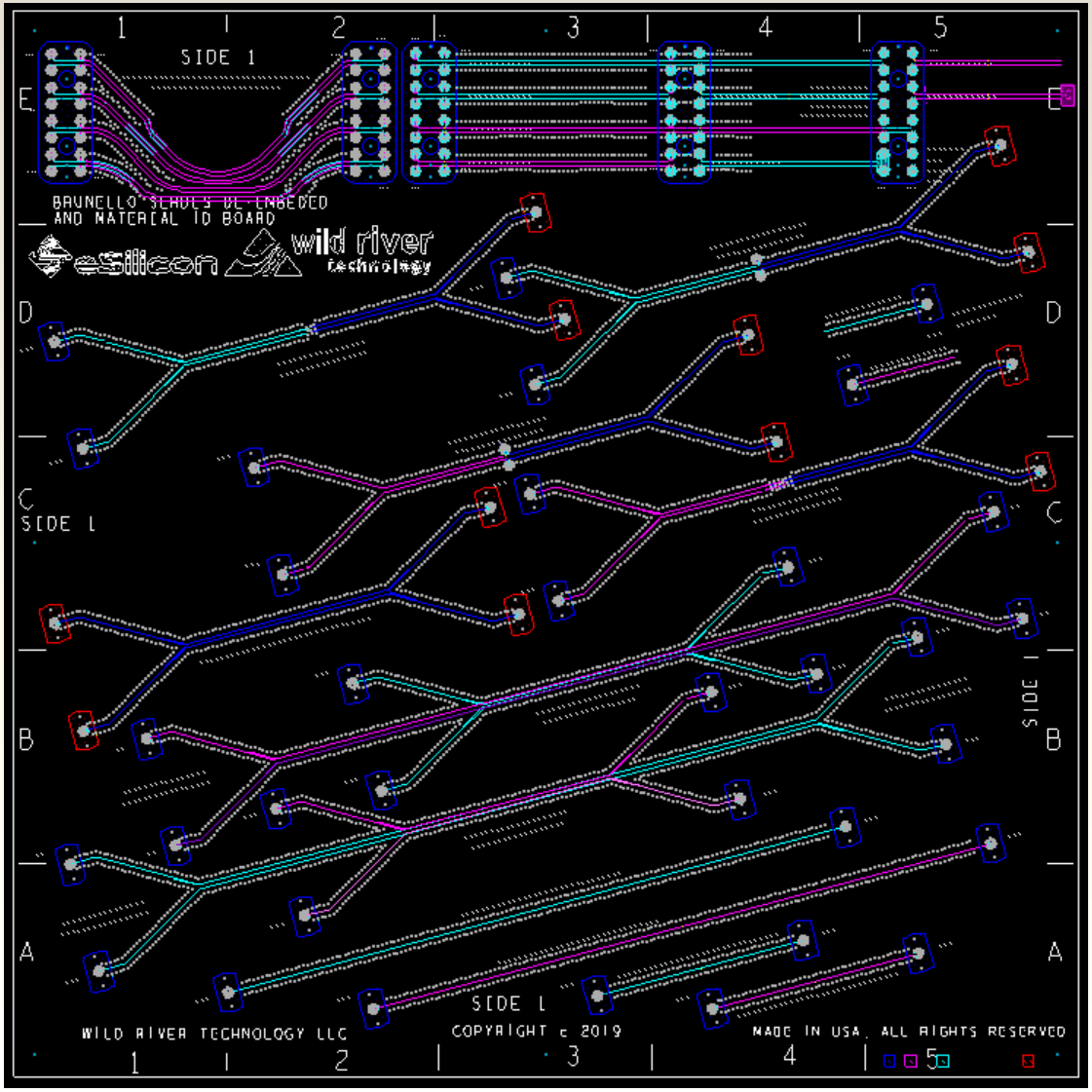


Time/Eye Diagram/Jitter

Let's do a Mind Experiment: What can go wrong with making SERDES measurement path?



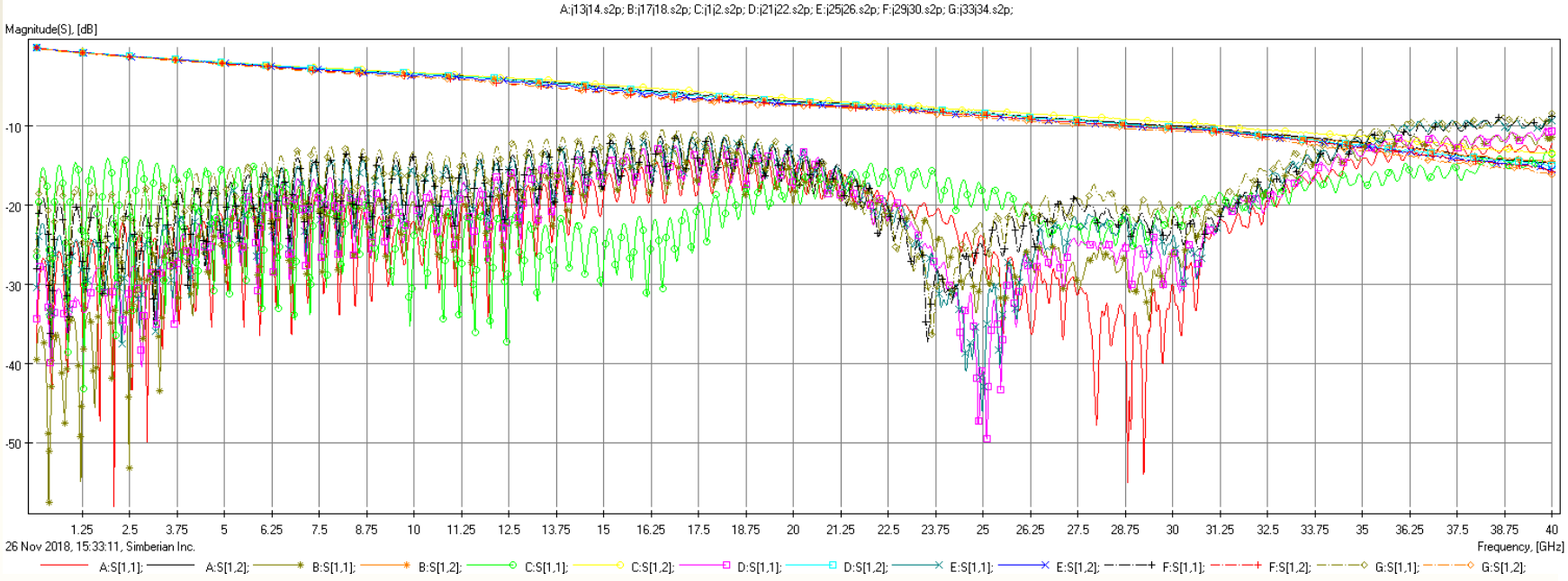
Let’s Identify Alamo Strategy examples



The Challenges of +50GHz SI

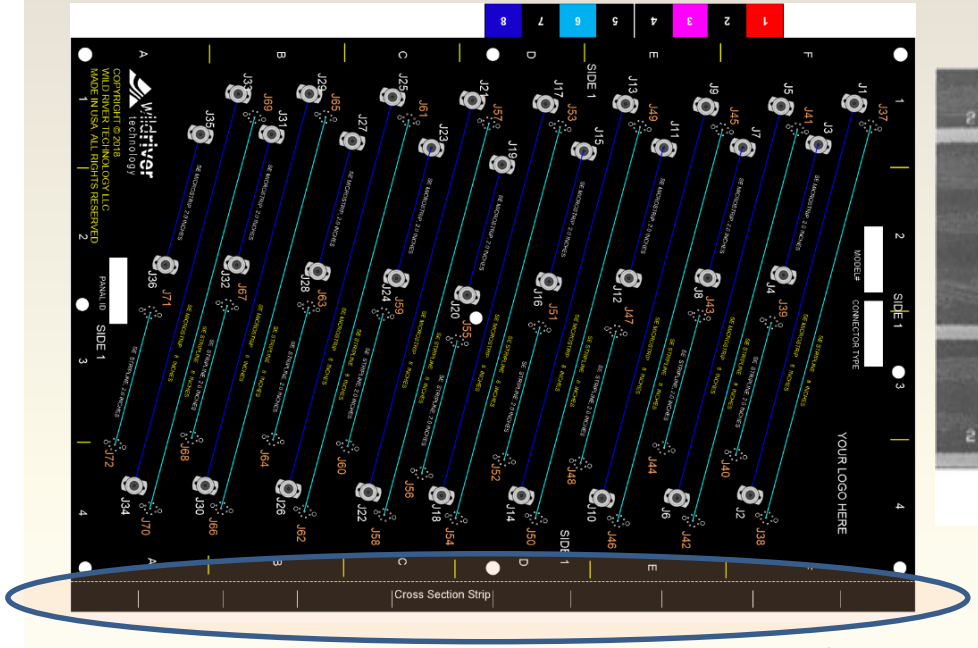
- EDA Tools and Simulation Methodology
  - Benchmarking the tool
  - Methodology and Tuning Your Simulation
- What Exactly is Good SI?
  - IEEE P370 TG1
  - How many spins to get there?
- The “Alamo Strategy” for Test Fixture Architecture
  - The Tale of 2 Titanic Captains
  - Always have a way out, the “Alamo Strategy”
- **The “Fabrication Hurdle” What is it, how to get past it**
- Why Program and Project Management gets in the way of 70GHz SI
  - Schedules versus Innovation and Building Technologies
  - Concurrent EDA Teams
- Closing Ideas
- Conclusion
- Open Discussion

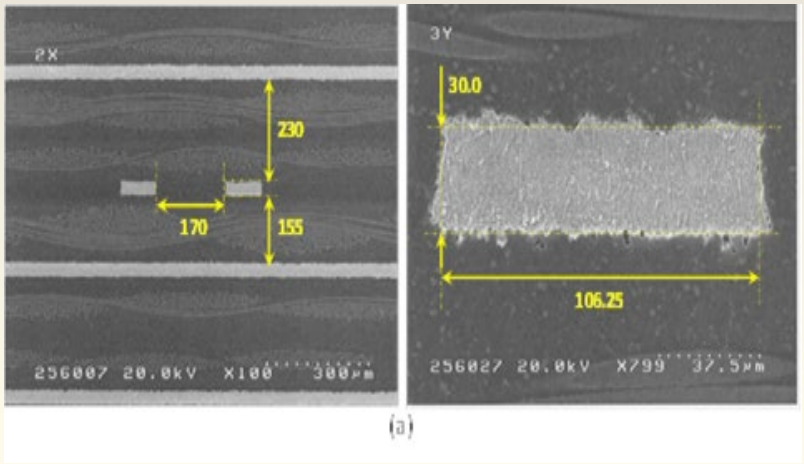
A 5-10% TOLERANCE DOESN'T WORK FOR STELLAR SIGNAL INTEGRITY



All 8inch traces in this plot are within 10% impedance tolerance

The Next Level of Signal Integrity: CMP-Beta-X and Cross Section





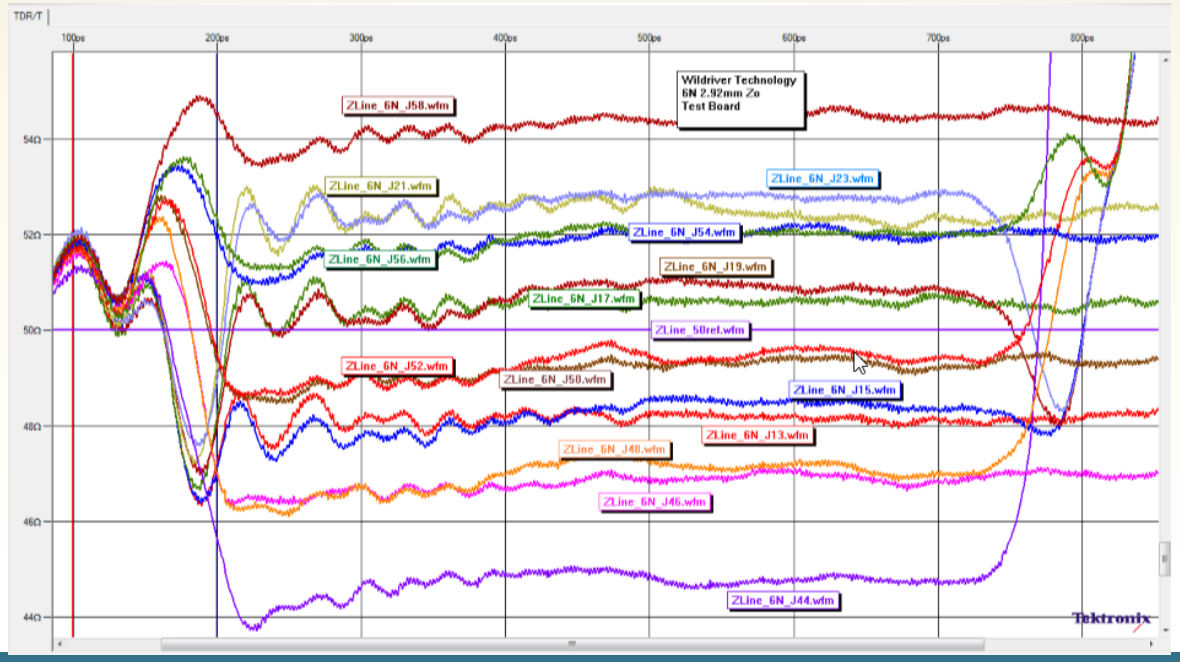
Cross sectional data is used for material ID and loss modeling

CMP-Beta established fine tune impedance, cross section, identifies fabgrication issues, resolves SI issue with fabricator, 2ohm system

Cross sectional analysis section

All Custom CMP-Beta include Cross Sectional Analysis for – Improves 3DEM analysis

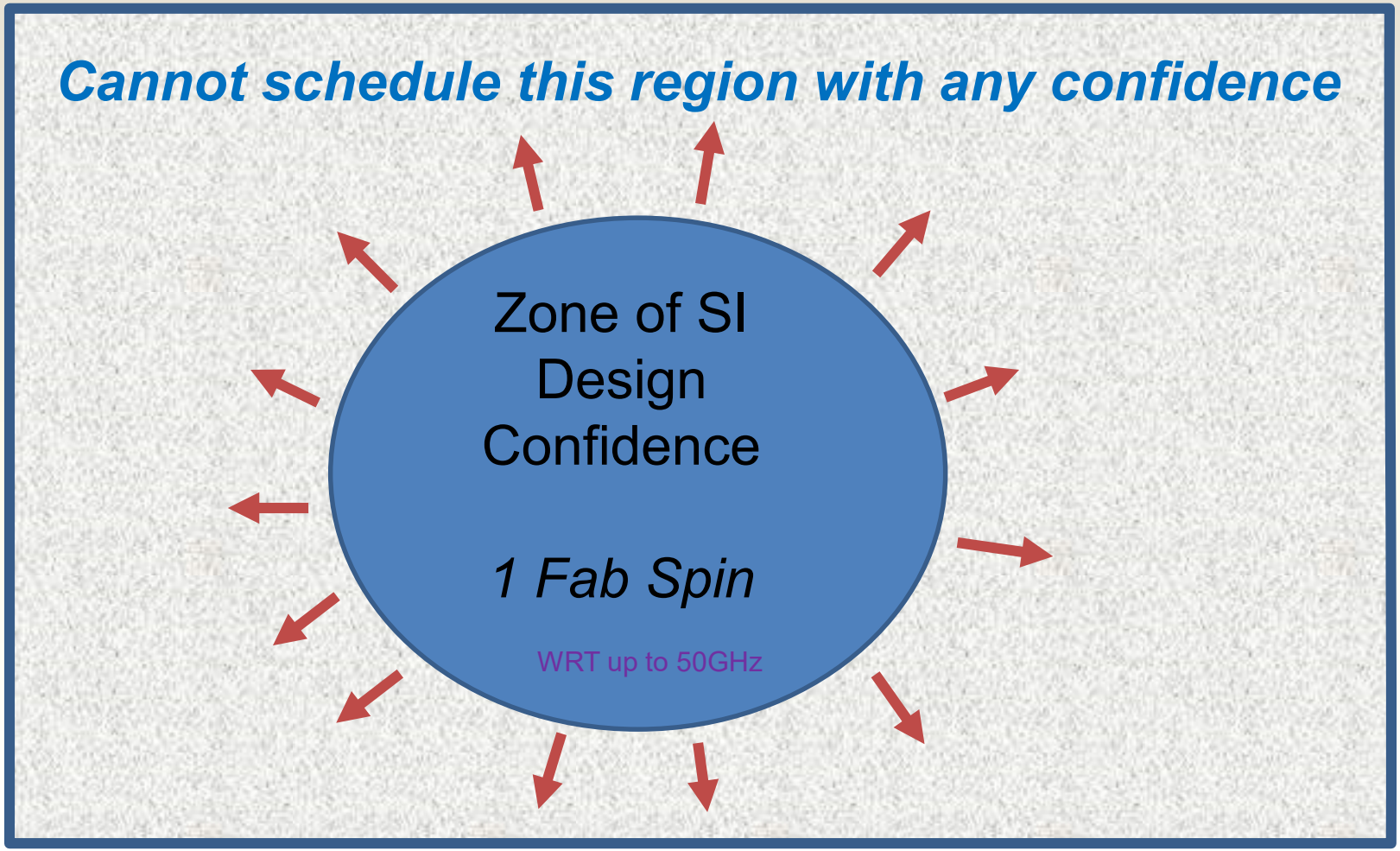
- Fabricators adjust things – NOT GOOD FOR SI!
  - Stackup adjustments
  - Etching and compensation for etching
  - Trace width and separation adjustments to "dial in the impedance"
- Optimal geometry selected and design as fabricated is firmly established
- ***Fabricator is now only manufacturer, not playing with your impedances or managing your SI!***



The Challenges of +50GHz SI

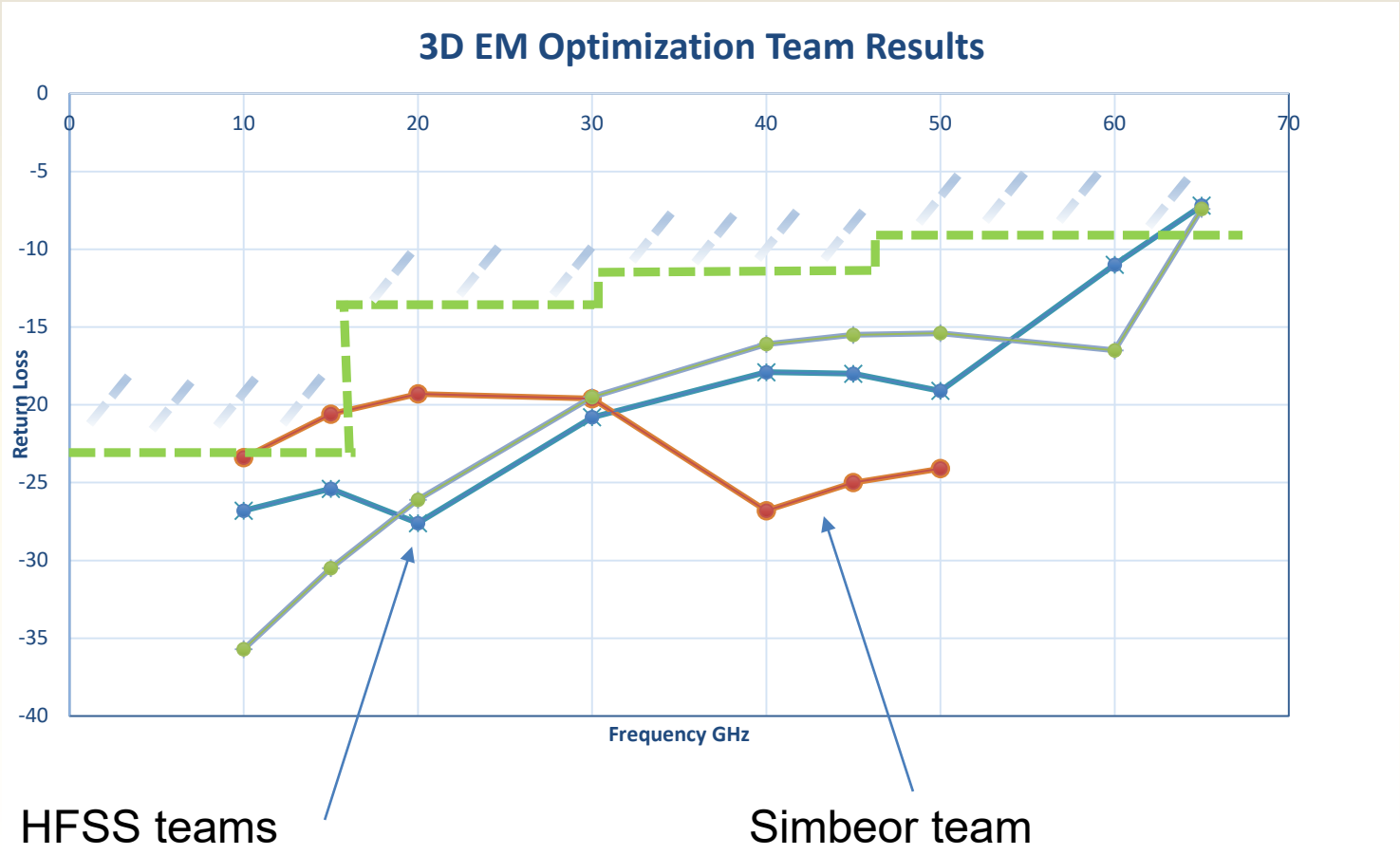
- EDA Tools and Simulation Methodology
  - Benchmarking the tool
  - Methodology and Tuning Your Simulation
- What Exactly is Good SI?
  - IEEE P370 TG1
  - How many spins to get there?
- The “Alamo Strategy” for Test Fixture Architecture
  - The Tale of 2 Titanic Captains
  - Always have a way out, the “Alamo Strategy”
- The “Fabrication Hurdle” What is it, how to get past it
- **Why Program and Project Management gets in the way of 70GHz SI**
  - **Schedules versus Innovation and Building Technologies**
  - **Concurrent EDA Teams**
- Closing Ideas
- Conclusion
- Open Discussion

Building Technologies and Innovating – Make Zone Confidence Bigger



3DEM return loss optimization goal and simulation results (green dash mask was targeted SI) – Result of 3 teams of engineers working independently

Mask (green dashed line) is based on PAM-4 power spectral density and IEEEP370 quality metrics



Conclusions - Review

- Be paranoid, have an Alamo Strategy
- Benchmark and tune EDA tool simulation
- Build Test Fixtures before Project Starts
- Establish clear SI metrics, use IEEE P370
- Manage the 10% Fabrication problem
- Fire the Project Manage, Hire Innovation Manager
- 3 EDA Teams
- Establish Sphere of high confidence design, increase sphere with innovation

Thank You!

- **Alfred (Al) P. Neves**
  - CTO at Wild River Technology
- al@wildrivertech.com
- 503-679-2429