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Free signal integrity? How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond

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Abstract

The “need for speed” in AI systems is driven by their requirement to process large data sets, both during training and application. Channel design is constrained by the balance between acceptable loss budget and the power consumed in equalization and error correction. Reducing channel loss can enable lower power or longer unrepeated channel lengths. Historically, high-speed serial links focused on material selection to manage attenuation. In 224 Gbps PAM4 systems, however, second-order factors like impedance variations, crosstalk, and power loss into cavities significantly impact the loss budget.

While identically similar virtual channels can be designed in simulations, real fabricated boards differ due to manufacturing variations and limited understanding of material anisotropy. As channel bandwidths increase to 56 GHz and above, accurately defining material behavior in simulations becomes crucial. This paper analyzes second-order design features using precision measurements of test vehicles and digital twins. We propose a metric-driven methodology based on AI/ML to determine relevant parameters for simulating anisotropic behavior that matches both time and frequency domain measurements.

When second-order factors are accounted for, it is possible to align our predictions from the simulation more robustly with the measurements of what was manufactured. In other words, the virtual design, aka the digital twin, allows us to predict the actual system performance more accurately. These digital twins, combined with AI/ML techniques, allow for design space exploration and sensitivity analysis to identify manufacturing tolerances and assists us in creating robust 224 Gbps PAM4 channels with acceptable total loss. The paper includes a study of the influence of anisotropy on the channel performance and examines methods to extract out the level of anisotropy. The overall goal is to achieve better than 2% measurement-simulation correlation in impedance profiles. This approach allows for optimized geometries and controlled geometry designs.

Author(s) Biography

Alfred P. Neves is the Founder and Chief Technology Officer at Wild River Technology. Al has 39 years of experience in the design and application development of semiconductor products, capital equipment design focused on jitter and signal integrity analysis and has successfully been involved with numerous business developments and startup activity for the last 17 years. Al focuses on measure-based model development, ultra-high signal integrity serial link characterization test fixtures, high-speed test fixture design, and platforms for material identification and measurement-simulation to 70GHz. He earned a B.S. in Applied Mathematics at the University of Massachusetts.

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John Phillips is a Senior Principal Application Engineer with Cadence Design Systems. Prior to joining Cadence John worked at many different companies covering such diverse marketplaces as high-end computer platforms and mil-aero. During his career he acquired a broad knowledge of SI, PI and EMC at chip, board and system level. John holds an MSc. Degree form Bolton University, UK. His current interests are SI/PI co-simulation and modelling for both serial and parallel interfaces.

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Eric Bogatin is a Professor at the University of Colorado, Boulder where he teaches undergraduate and graduate courses on signal integrity and system design. Additionally, he is the Dean of the Teledyne LeCroy Signal Integrity Academy, at www.beTheSignal.com and a Fellow with Teledyne LeCroy. He is also the technical editor of the Signal Integrity Journal

Introduction

The current and next-generation high-speed serial link systems are pushing up against the fundamental limits of the physics of the interconnects. Two features set the highest bandwidth of an interconnect: the insertion loss at the Nyquist and a resonance-free monotonic drop-off in the insertion loss. A monotonic insertion loss can be compensated with equalization as long as the insertion loss is above about -35 dB at the Nyquist. Resonant features that cause ripples in the insertion loss set the fundamental limit to the effectiveness of equalization.

Driven by time-to-market requirements, there is a constant pressure on the SI engineer to sign off a design without adequate knowledge about the vendor's PCB fabrication process and the laminate system. Therefore, they make assumptions about the PCB geometries using the layout as-designed data (from ECAD), the PCB material properties based on material vendor data or qualified estimates along with the PCB fabricator's confirmed stack up; what is the impact on risk and cost of this approach?

Below is an example of such a process showing the predicted insertion loss and return loss of an 8 inch stripline channel (red) vs the measured manufactured PCB (green). The s-parameters are full-path, i.e. non-deembeded, with the reference plane at the coax mating plane. While the return loss shows excellent agreement, the insertion loss is significantly underpredicted, which has implications for the channel performance.

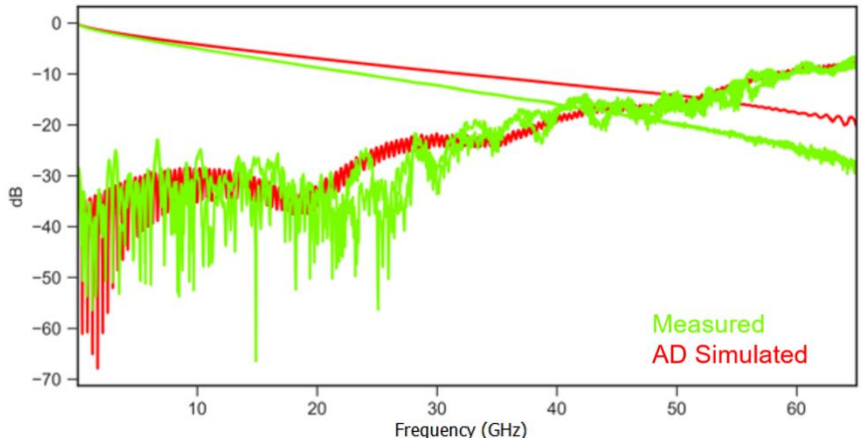

Figure 1 As Designed simulation to measurement correspondence. Green is measured manufactured board and red the As Designed simulation results.

With higher losses, either more complex equalization and/or FEC is required, which translates into higher overall system cost and power consumption. With most current design approaches, a significant simulation margin of about 5-10 dB of insertion loss at the Nyquist must be added, the exact figure depending on the workflow, confidence in the simulation tools and simulation setup, the PCB vendor's capabilities, and the risk aversion of the designer. Reducing this simulation-to-measurement gap, can recover design margin and reduce the cost of a system pushing the limits and in turn, leads to a more cost-effective system.

In this paper we explore a process based on detailed simulation and measurements to examine some of the challenges in reducing the gap between simulation and the manufactured design to achieve a more robust system. In this process, we will examine the influence of material modeling approaches, such as the difference between bulk isotropy and anisotropic assumptions, and manufacturing tolerances on the modeling process and performance.

Reducing the Simulation Margin Budget

The final metric of the simulation margin is the expected worst-case difference between the simulated behaviors of the digital twin and the fabricated structures. While it is the BER of the channel that is finally compared between the real interconnect and the digital twin, an initial approach is to compare the frequency domain behavior of a channel as measured and the as designed extracted model from the digital twin.

The electrical behaviors are captured by the S-parameters of the channel. For a differential channel, this is a 4-port S-parameter matrix, which should be evaluated from low frequency to above the Nyquist frequency, which is 56 GHz for a 224 Gbps PAM4 application. For crosstalk evaluation, an 8-port S-parameter matrix or clever port connections and terminations are required with a 4-port measurement.

The S-parameters contain all the important electrical behaviors of a channel and can be displayed in the frequency domain and the time domain. In addition to the magnitude and phase of each S-parameter, other important behavioral metrics are:

- The dispersion curves in the form of the time delay of each through-path, which can be derived from the unwrapped phase of the insertion loss
- The TDR response of each port to reveal the spatial variation of the instantaneous impedance
- The near-end crosstalk in the time domain to reveal the spatial location of the coupling
- The near-end mode conversion to reveal the spatial location of the reflected mode converted signal

It is also important to recognize that simulations can only be done with as designed (AD) channels, and measurements can only be performed on as fabricated (AF) channels. The goal is to reduce the simulation margin between a digital twin of the channel and the measurements of an AF channel.

The differences in the features between the AD channel and the AF channel include all the material parameters and geometry properties, such as Dk, Df, copper conductivity, copper roughness, the trace line width, the dielectric thickness of each layer, the thickness of plated copper, and the finished via drill hole sizes. The differences between the AD and AF parameters have two parts:

- The difference in the fabricated geometry features vs the geometries used in AD
- The manufacturing variation in each AF feature and their statistical distribution

As an example, given some etch back, the AF line width will be different from the AD line width,and will also apply to capture pads and clearance holes through planes. The uncertainty of the drill location will affect the position of the vias relative to their clearance holes. Layer to layer registration effects the clearances around vias, alignment of slots and gaps and the like. An example of a via cross-section shows some of these natural real-world AF variations is shown in Figure 2, dotted vertical lines have been added to make it easier to see the layer registration error, but also plating and etching variation is visible. How well the features of the AF structure are replicated in the digital twin will affect how well the measurement corresponds to the simulation and hence the margin for instance in the insertion loss and TDR response.

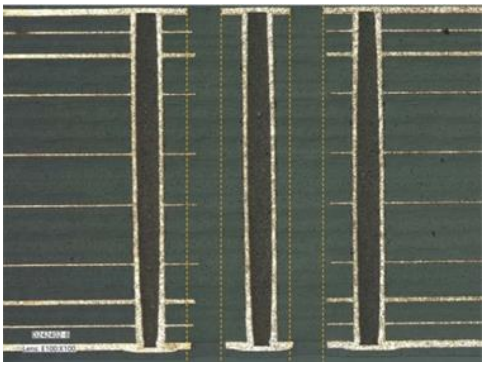

Figure 2 Example of a cross-section showing nonuniformity in via cross section, variable hole clearance size and registration.

A starting place in reducing the simulation margin is to use a simulation tool that includes important real-world effects such as causal material properties, anisotropic dielectric properties, and copper roughness models. An added plus is also the versatility to quickly explore design space to find the optimized values of the AD geometry, model and materials that match the AF values. When the AF parameters are known and used in the simulation to replace the AD parameters, the digital twin should show a better, optimized match to measurements.

Reducing the simulation margin and improving the measurement-simulation correspondence have been the goals of the industry for many years. A common method is measurement-based model extraction, which is the process of optimizing the AD features of a digital twin until the simulated S-parameters of the digital twin match the measured values of the measured channel..

In this study, we focused on exploring the use of test structures to extract material properties and their sensitivity to anisotropic material properties.

We found that the combination of five factors, all convolved together, contributing to the simulation margin:

- The Dk and Df of each layer
- The inhomogeneous distribution of otherwise uniform materials
- The anisotropic properties of the Dk of each layer
- The manufacturing variations and the difference in the geometry of the AD and AF structures.
- Non-uniqueness in the measurement-based model extraction of the AF features

To unscramble the interactions of these five factors requires designing structures that have specific S-parameter matrix elements that are more sensitive to one of these factors than the others. Then, a combination of multiple test structures and an optimizer are used to simultaneously explore design space to find the optimized AD features such that the digital twin simulation matches the measurements. This is a long-term study.

In this early phase, some of the elements of this long-term study were evaluated. In particular:

- A new well-characterized test vehicle
- An optimizer with AI and ML features to efficiently explore design space and identify material models for use in simulation
- The sensitivity of some structures to anisotropic materials properties

A Well-characterized Test Vehicle

Channel Modeling Methodologies for Material Identification

A Channel Modeling methodology utilizes advanced test vehicles to address virtually all crucial high-speed signal integrity issues. An area of focus for such methodology is on fitting EDA material models and then verifying these models against a set of reference structures. One objective of this section is to outline some of the practical considerations of improving our digital twin and identify parameters to use to better match the AF measurements.

A secondary objective is to address the related requirements of not having to do de-embedding of the launches as it is the authors experience that the de-embedding procedure can add noise , in particular, to the phase response used for identifying the material models to use in our digitial twin. In order not to require de-embedding the hardware platform should have:

- Virtually perfect RF launch design
- Consistency from launch to launch to avoid any residual issues due to SI or connector placement
- Measurements that have adequate return-loss calibration margin in order to maximize the separation of RL to IL by reducing the RL uncertainty.
- Management of all transitions, including single-ended to differential signal transitions

Introduction of the Test Vehicle, CMP-70

The CMP-70 (Channel Modeling Platform) Test Vehicle, shown in Figure 3, was used for this study. It is a 70GHz platform used for material model identification and fitting and RF launch optimization via design and differential analysis. It includes a cross-sectional analysis that provides a direct measure of the geometries needed for As-Fabricated material identification.

Figure 3 The Wild River Technologies CMP-70 Channel Modeling Platform

The important CMP structures suited for material identification fall into two rough groups (not addressing microstrip differential or mixed-mode model fitting important for analysis of the solder mask): structures used for extracting a model and structures used for verification of the models. Model verification for a particular EDA tool serves to provide unimpeachable confidence for high-speed design (HSD), which includes full material ID in both in-plane and out-of-plane material properties suited for HSD greater than 10 Gbps. The structures utilized in this project are listed in the table below.

RF Launch Connection	Structure Used	Comments and Function
J1-J2	2" Microstrip	Solder mask and prepreg material ID, used with 8inch using GMS methodology to isolate 6inch of de-embedded transmission line
J3-J4	2" Stripline	Core prepreg material ID, used with 8inch using GMS methodology to isolate a 6inch of de-embedded transmission line
J9-J10	8" Stripline	See 2 inch stripline comments
J11-J12	8" Microstrip	See 2 inch microstrip comments

J27-J28	Beatty Class Structure, 50/60/50Ω. Stripline	Impedance verification analysis
J62-J63	Anisotropic Resonator	Used to determine X-Y and Z-axis Dk material model fit
J77-J80	Microstrip Differential Thru 6 inches, 100Ω	Used for determining Solder mask and prepreg Dk, Df. Coupled microstrip has high field density between coupled lines which improves model fit analysis of solder mask. Not crucial for HSD.
J81-J84	Stripline Differential Thru 6 inches, 100Ω	Differential stripline is impacted by both X-Y, Z-axis, and fringing fields (both axis effects) so represents excellent verification structure of X-Y/Z axis model fit

Table 1: Structures utilized.

Description of the CMP-70 Stackup

The CMP-70 stack up was designed with Isola's Tachyon 100G material. Tachyon 100G laminate comes standard with spread glass and smooth copper HVLP (VLP2) that provides a platform to mitigate skew and minimize loss. The nominal low Dk of 3.02 and Df of 0.0021 provide a platform for long-reach channels operating with Nyquist of 56GHz or below. The different laminate constructions have variation in the Dk and Df values due to glass weave and resin content, these need to be considered for the target designs' stack-up. The material is compatible with HDI (High Density Interconnect) technology applications, allowing multiple lamination cycles for the designs utilizing fine-pitch devices. The stackup for the test platform is shown below in Figure 4.

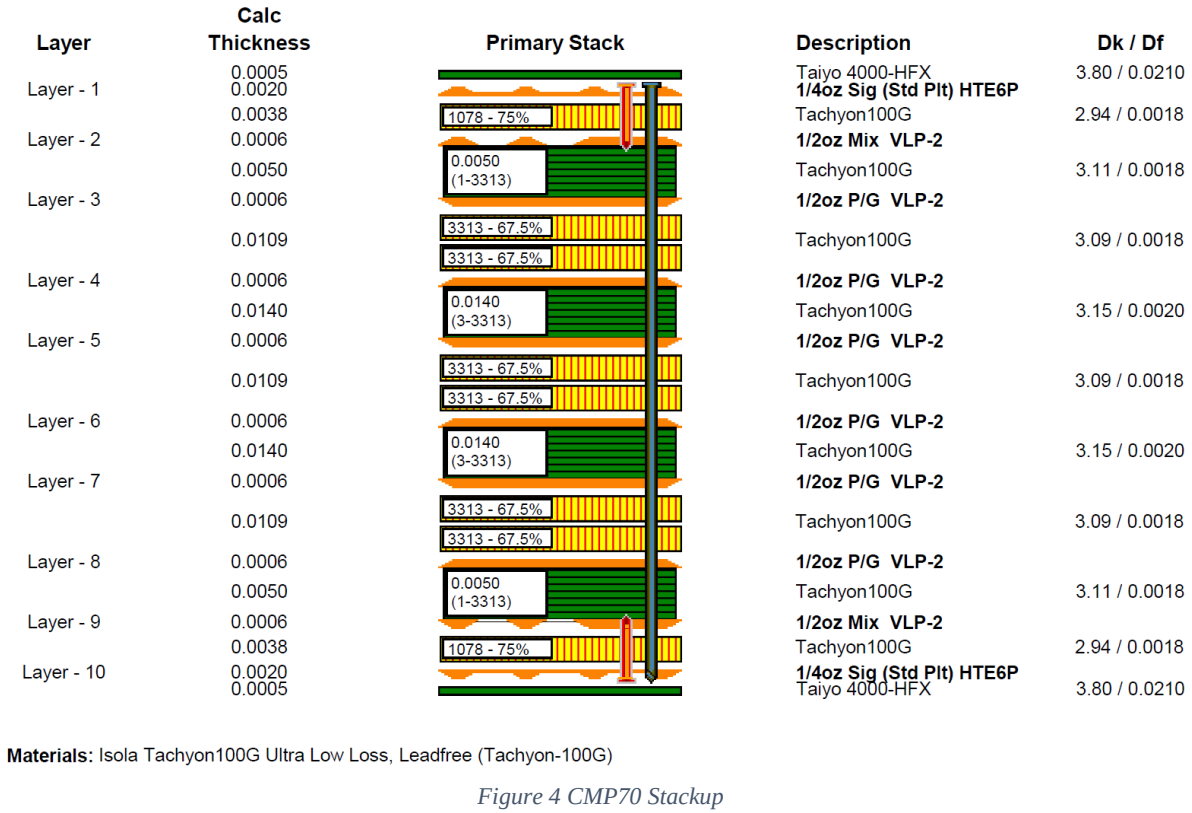

Figure 4 CMP70 Stackup

The core layers of the stack-up use multiple ply of 3313 glass based laminate to provide rigidity in the test platform and can be replaced with different constructions for power and lower-speed signal application layers.

The spread glass laminate 1078, shown in Figure 5 provides the compatipility with HDI technologies. The 1078 75% prepreg used fits within the standard Design for Manufacturing (DFM) applications for HDI and provides a nominal 50Ω Microstrip impedance line width of 5 mils facilitating reduced loss and increased channel reach.

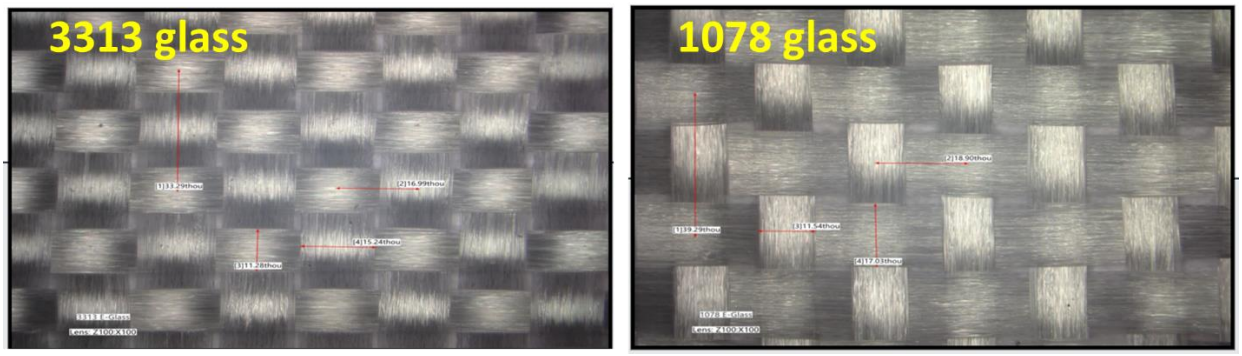

Figure 5 Examples of the glass styles for different layers, courtesy of Isola R & D Laboratories.

It is important to work with the fabricator to make the appropriate selection to maintain the required layer thicknesses based on the copper layer percentage and the fabricator's pressing characteristics.

The stackup layers 1 and 2 (symmetrical with layers 10 and 9) can be replicated with multiple lamination cycles to provide an increase in layers used for high-speed signals. This stack-up provides good localization of the signals with no large gaps between the layers reducing crosstalk and jitter susceptibility. The CMP70 style and method of stack-up provide a good starting basis for general high-performance designs through 70 GHz.

Channel Modeling Platform Considerations for Material Identification

There are numerous key signal integrity issues related to high-confidence material identification and model development. A common approach when building advanced test vehicles is to use a de-embedding tool to remove the connector artifacts. This approach is plagued with issues, mostly a considerable reduction of usable bandwidth and a reduction of simulation-to-measurement correspondence.

The approach in this paper is to use a General Modal S-parameter methodology to extract the bulk Dk, Df and then afterwards to check the quality of correspondence to measurement using full path extraction (i.e. including the connector launches). The fit with measurement was validated amongst others using a Beatty class structure. The Beatty standard structure using a 1W-2W-1W (50/25/50Ω) is shown in Figure 6. The outer lines show full path reference planes, which include the RF launches, versus the de-embedded reference planes placed 70 mils from the low impedance region.

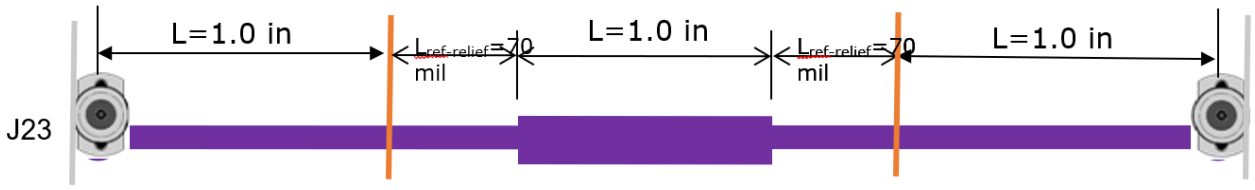

Figure 6 The Beatty Standard CMP-70 structure with the reference planes identified.

Connector Launch Design

Optimizing the connector launch with low enough return loss so de-embedding is not required starts with choosing a connector with high enough bandwidth, and then optimizing the pad stacks and clearances of the launch. Engineering a coax to PCB launch with low enough return loss so that de-embedding is not required means attention to seven features:

1. The measured return loss, using AF features and simulated return loss, using AD features, needs to be low, so that there is significant margin between insertion and return loss
2. The vectorial difference between the return loss floor of the measurement needs to be significantly lower than the measured return loss to minimize the vectorial error of the measurement. Return loss vectorially impacts insertion loss (Dk and Df fit), and the return loss relates to the transmission line impedances, which are used to verify the Dk fit.
3. Both micro- and macroscopic signal integrity needs to be addressed.
4. Considerable mechanical care of connector placement needs to be done to satisfy 3. Connectors should be installed with fiducial alignment tabs. Mounting should be done with two wrenches and correct torque, so the connector pin is aligned with via pad.
5. The connector models need to be tested.
6. Coaxial connectors are single-ended launch. Single-ended to differential transition of transmission lines requires careful EDA optimization and signal integrity design to maintain both low single-ended and differential return loss.
7. Microvias are typically required for frequencies above 50GHz, connector launch pad to signal via pad alignment is critical also for item 3.

All above practices were observed when adding the 1.85mm vertical launch feed connectors (Samtec 185-J-P-VP_ST_CM and 185-J-P-VP_ST_CMM). A simple test of the connector model can be done by simulating two connectors back-to-back, as shown in Figure 7. While this is not the intended application, it can give some insight into the quality of the connector model. The TDR response shows less than 2Ω discontinuity from the 50Ω coax at 7.5 ps rise time. Note that the response is slightly inductive by design, and this helps to mitigate the excess capacitance of the PCB. The image is from previous work discussing the proper placement of ports on the connectors and doesn't represent the connector used on CMP70 [1].

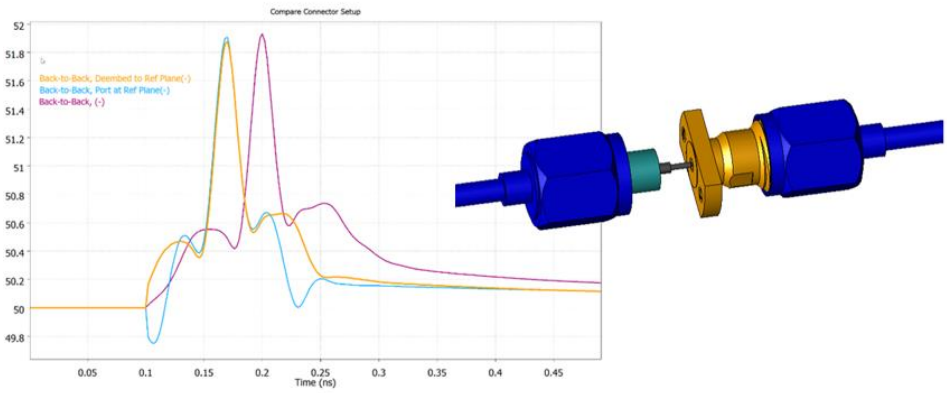

Figure 7 . Sample exploded view model of two connectors mounted back-to-back and the TDR response of the back-to-back connectors. The higher peak inductance of the pin counters some of the capacitance of the pad when mounted on the board.

Reducing the simulation margin of differential (DIFF) versus single-ended (SE) interconnect regions pose additional challenges. SE to DIFF transition designs must result in low SDD11 / differential return loss. Launch design must also be pristine, along with skew and mode mitigation by designing the differential trace on the glass-glass pitch and/or rotating the signal trace path relative to the glass weave direction, as is done in the CMP-70. Figure 8 shows the transition from the SE coax launch to the coupled region of the differential pair.

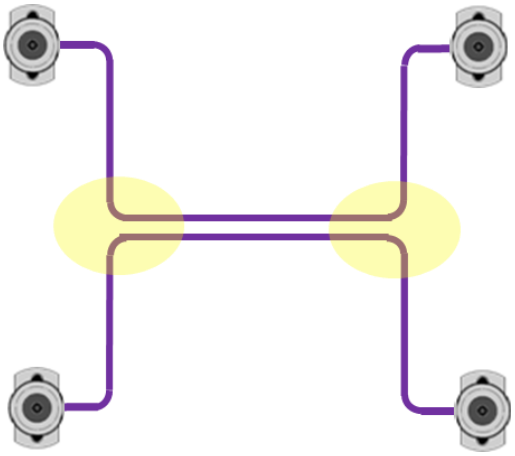

Figure 8 Example of a single-ended to coupled transition with SE to DIFF transition regions highlighted

There are numerous practical mechanical and pin-alignment issues related to compression mount vertical launch connectors to achieve a nearly transparent launch. This connector utilizes two wrench locations for mounting cables to minimize torque as shown in Figure 9. A secondary (illustrated with yellow highlight in the middle) SI consideration is alignment cutouts in the connector body that serve to improve signal integrity by aligning the connector pin on the signal pad using PCB fiducials.

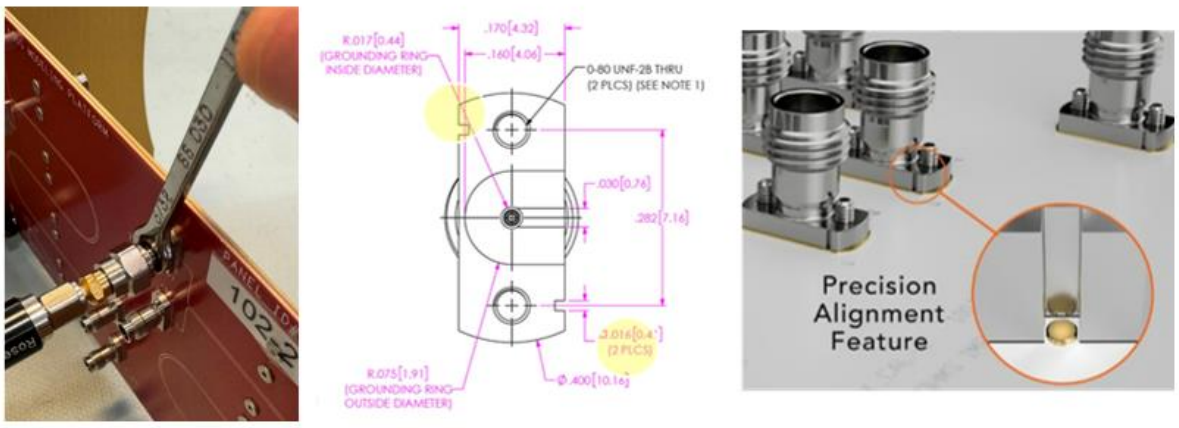

Figure 9 An example of proper care in using the SMT connector to maintain good alignment with the signals.

Signal Integrity - Macroscopic Versus Microscopic

Normally we just talk about signal integrity, however this covers so many aspects that we often forget some important factors. For this reason, we are in this paper distinguishing between two levels of signal integrity – macroscopic and microscopic.

Microscopic SI focuses on isolated structures, or full path SI for a single channel at a specific location of the board. Comparing what we measure for such channel vs what we simulate is often thought of as validation, but it neglects a very important parameter – the nature of manufacturing and variation of launch connection, and material variation. For instance, Dk across a panel can vary by as much as 10% and there is pressing thickness and line width variation etc. In other words, having the exact same structure replicated through a board, we will not see the exact same behavior – we can expect variation. Considering spread due to manufacturing and materials and looking at SI in a more holistic context is what we call **macroscopic SI**.

An example of the differences between the micro and macroscopic properties of a launch is shown in Figure 10. The differential TDR measurement is with a 7.2 ps rise time and shows the connector, the connector mounted to the circuit board, the launch into the single-ended region, and the nearly transparent transition to the coupled region.

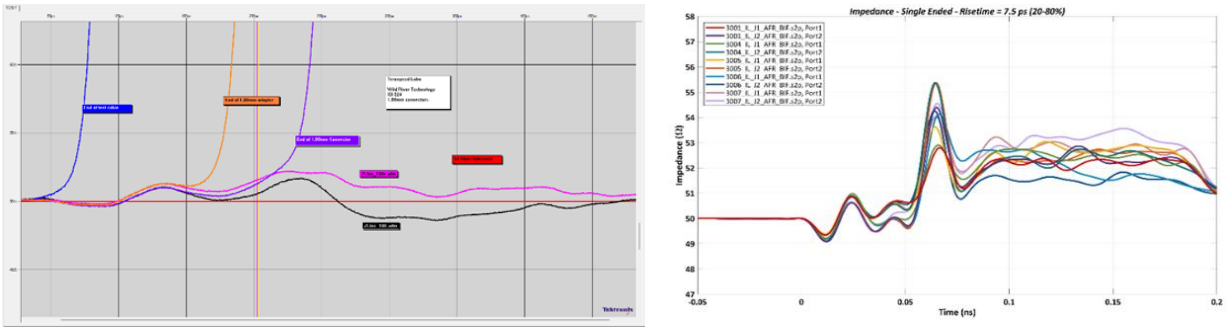

Figure 10 An example of microscopic vs macroscopic launch design. On the left, the measured differential TDR of the connector, the connector to the board, and the transmission from the SE region to the coupled region. On the right an example of macrolevel signal integrity where connector quality is tested by measuring the TDR response of multiple nominally identical launches.

Figure 10 also shows an example of the typical variation of the connector launches and transmission lines that are nominally identical. By looking at the spread of the impedance we can

better understand the overall behavior of the system and of course it is the job of the SI engineer to take spread into consideration when defining whether the channels on the board are reliably within spec. In simulation we mostly simulate only nominal structures and so understanding the spread is critical to a products' viability.

To improve the digital twin and hence the level of predictability in our simulations, we need to update the simulation model with inputs from what we manufacture (AF parameters). The dimensions can be updated with information from the manufacturers cross section report. Figure 11 shows an example of one such cross-section from which we can gather information about etching, trace widths, layer heights, solder mask thickness etc. These AF parameters differed from the AD parameter values shown in Figure 4. Further screen shots of important aspects are shown later in the paper.

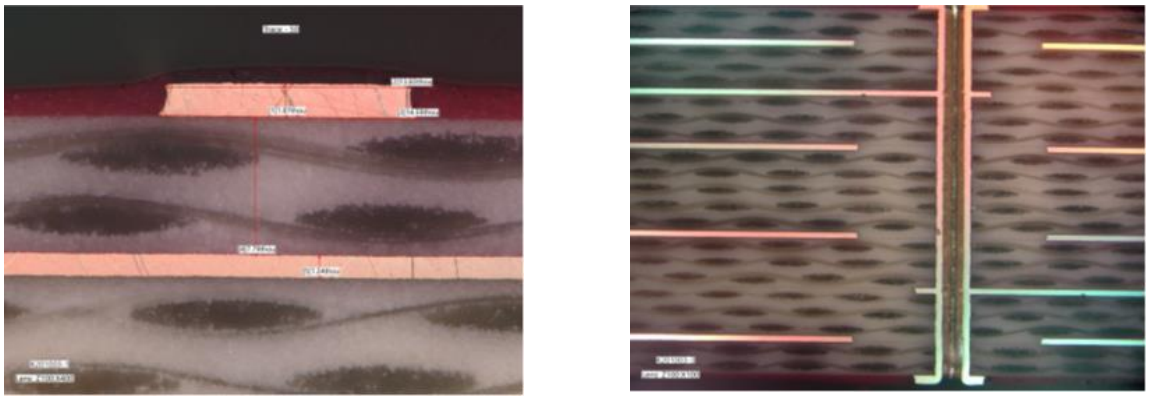

Figure 11 Cross-sectional analysis reports are used to confirm the as-fabricated (not as-designed) geometries for import into EDA tool for identification of material identification models

As can be expected from the high-quality manufacturer used for fabrication of this design, inner stripline traces show little etch back, and the etch factor was close enough to 90 degrees that the trace widths could be simulated with the as-designed width values. The microstrip traces show more variation in the plating thickness and the resulting trace geometries, PCB manufacturers are required only to meet minimum plating thicknesses depending on the PCB "class" [2]. Considerable variation in the solder mask thickness was also noted; this, coupled with the effect of the plating, leads to large uncertainty in the final microstrip trace impedances and their effects on other test structures.

Note, that cross sections are mostly only available from a test coupon and not the structures on the actual board, thus some additional variation can be expected between what is simulated and what we measure. However using the properties, we get from the cross section at least provides a better starting point for an improved match with manufactured design. We will be using structures on the CMP-70 board both to identify material properties and to verify that the identified materials match other structures across the board. How much variation we see in simulation vs measurements provide us valuable insight in the sensitivity to second-order factors such as manufacturing variation, material uniformity, and dielectric anisotropy. That is, we can test whether our measurement-based model provides a good macroscopic fit. As different structures have different sensitivities to the second order effects we can potentially use some of these structures for understanding the in-plane vs out-of-plane Dk, manufacturing tolerance sensitivity and so on. In this way we might hope to gauge the uniqueness of the identified AF properties we use for simulation. Bare in mind, that it is possible to create models that meet some aspects of the solution space but fail to align with measured data in other scenarios.

Extraction of Material Properties

We saw in the beginning of the paper how far off we could potentially be with our as-designed simulation setup so to improve the fit with the fabricated board we will use structures on the test board to identify the material models to use. We will start by assuming that the materials in the stackup are homogenous as this is the most commonplace modeling practice. This is what we term bulk material properties. We will then afterwards look at structures to use for identification of anisotropic material properties.

Bulk Material Identification

In this section we will assume that the dielectrics are completely described by an effective isotropic permittivity value, Dk, and loss tangent Df. To ensure causal behavior we also must consider frequency dependency of the dielectric. One such model is the Djordjevic-Sakar [3] model which has 3 other parameters of importance: the lower and upper cut-off frequencies as well as the base frequency. For the sake of simplicity, we chose 1 GHz as the base frequency because that is typically available in datasheets, and for the upper and lower cut-off, we used the tool default of 10 kHz and 160 GHz, respectively.

For capturing the frequency dependent effects of surface roughness a Huray [4] model consisting of a 3-ball stack, after [5] with equal size spheres and fixed surface ratio to 4.887 leaving only one variable for the model – the nodule radius r. These assumptions are identical to the those made in previous work on an earlier version of the test platform and thus conclusions and simulation results here can more or less be directly compared [1].

When we try to identify material models, whatever method we use, the material identification will need to map information about the AF features to the simulation model. Models commonly used in EDA tools today do not take measured parameters directly as input. This information is difficult to translate literally into a digital twin. Also, we need to keep in mind that we are essentially trying to simplify the problem ro be a deterministic one while it actually is not – material buildup, resin content, surface roughness profile, PCB manufacturing variation such as, trace width, etching, pressing, and drilling are all aspects that have non-deterministic statistical variation across a single board instance, across boards in the same batch and across batches and as such we need to bound the problem rather than treat it deterministically.

In addition, during operation, temperature, humidity, aging, etc., cause variation, so although a very detailed physical model gives us unique engineering insights, they may lure us into dealing with the problem as if it were deterministic. Also, there is a big difference between modeling for microscopic agreement and having analysis that accurately predicts the macroscopic performance considering tolerance and variation. The platform used here allows us to gauge variation across an entire board for several relevant metrics.

One of the additional challenges we have to contend with, as highlighted in multiple references such [6], [7] and [8], is that the material identification process is not unique. We can end up with multiple solutions to the model parameters that produce practically identical or near identical system responses.

For instance, surface roughness impacts the delay through a transmission line as does the dielectric constant itself, and losses are contributed by both the metal and dielectric. The losses are somewhat separated in frequency (skin losses scales with sqrt(f) while loss tangent losses scale with f), but careful simulation and test platform measurement setup is required to separate them. The eggs have, so to speak, already been scrambled. Howeve, in the end you want to ask yourself, do we

really need to care about the exact models or parameters if they allow us to replicate the terminal behavior and the impact on the eye-diagrams?

In our previous work on the predecessor to the current test platform [1], we did manual material identification based on sweeps and a 3-step procedure. In this work we applied an AI/ML optimizer [9] directly extracting all material properties in one shot. In this process, we needed to identify surface roughness for both plated and unplated layers, core and prepreg dielectric constants and loss tangent. To achieve our goal a set of 250mil long traces were parameterized (both materials and geometry), these were excited with wave ports to allow us to match to the measured transmission line segments. These measured results were derived through mathematical transformations from the measured data, which was described in the previous paper [1].

Additional unknowns are present that could be added to the optimization, but which were assumed fixed in this case. Specifically, we needed a material identification for the microstrip layers, which are notoriously plagued by issues related to plating thickness, etch factor, controlling the dielectric heights, and solder mask variation. Figure 12 shows a close-up of the stackup, which was used for initially identify the isotropic material properties.

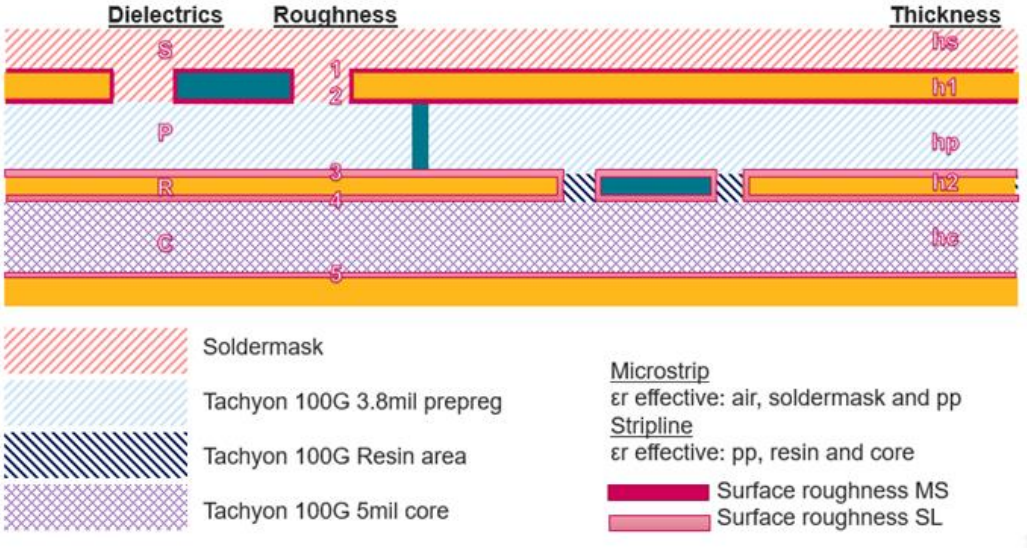

Figure 12 Stack up for the microstrip line with the features to be optimized.

The material system being identified is quite well matched in terms of the electrical performance between core and prepreg. Principally these could have been treated as one homogeneous dielectric for the stripline layer, however, we chose instead to separate identification of core and prepreg properties because only the prepreg and solder mask contributes to the microstrip layer performance. It was also a desirable outcome to be able to identify material properties that can be re-used when using the same material in other stackup configurations. However, we believe, without having exact proof at this point, that reusing the identified material properties for the given buildup may not necessarily give you the result fidelity you need so if you are going in that direction, proceed with caution!

For the present case, we will assume the solder mask height and material properties based on input from the PCB manufacturer are in line with the data available in the as-designed process. Material identification was done with varying copper conductivities based on defaults as well as from previous experience. In either case, the resultant material models identified were more or less identical because of the large frequency band used for the optimization, where it is way more important to get surface roughness right. However, if matching the trace performance in the low

frequency range is important, then the appropriate copper conductivity value should be identified first.

Separate surface roughness models were created for the outer plated layers vs the inner layers in the PCB, as higher roughness copper was used as the base layer for plating. From Figure 12 above, it is clear that we could choose arbitrary levels of detail and variables to describe even just the 3 outer most layers of the design. Figure 13 summarizes the assumptions made with the properties to be optimized boldfaced.

	Height	Conductivity [MS/m]	Dk_{avg}	Df	Surface roughness, r	Surface Ratio
Solder mask	X section	NA	Datasheet (3.8)	Datasheet (0.021)	NA	NA
Layer 1 (HTE)	X section	58	Solder mask	Solder mask	r_{outer}	4.887
Prepreg	X section	NA	$Dk_{avg,pp}$	Datasheet (0.0018)	NA	NA
Layer 2 (HVLP2)	X section	58	Prepreg	Prepreg	r_{inner}	4.887
Core	X section	NA	$Dk_{avg, core}$	Datasheet (0.0018)	NA	NA
Layer 3 (HVLP2)	X section	58	NA	NA	r_{inner}	4.887

Figure 13 Assumptions for bulk material identification

For optimization, we need to indicate what variables we want to optimize, their ranges, and the goal function to drive the optimizer. In addition, of course we need to choose the frequency range over which to optimize. For the Dk ranges, we used the datasheet dielectric values and extended the range by +/-10%. For the surface roughness, we obtained estimates for Rz based on [10], [11], and used this to set the initial nodule radius and let the optimizer vary r up to a value of 0.262µm (which was used for the previous generation platform which had less smooth copper foils). We set the goal function to compare the complex insertion loss for both the microstrip and stripline against the corresponding measurement data. The error was described as a relative root-mean-square error, RMSE, over the frequency range of interest, in our case from 0-50GHz.

Figure 14 displays the output of the simultaneous optimization of stripline and microstrip structures.

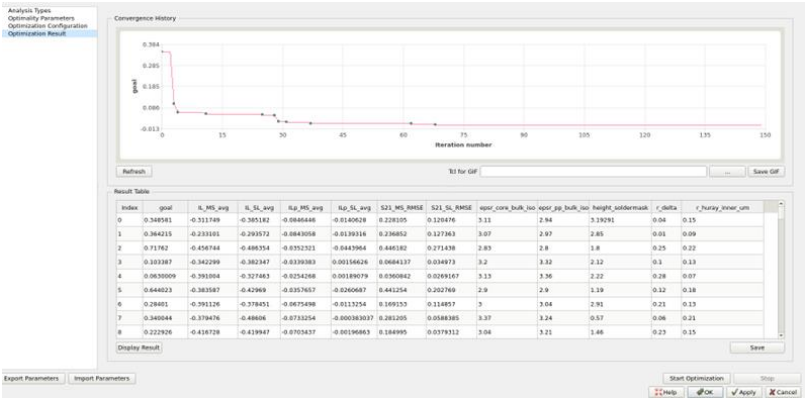

Figure 14 The convergence of the relative root mean square error as the optimizer searched design space

You will note in this case that the optimizer goal function shown in the upper half of the screen capture converges within less than 30 iterations. The general finding with this AI enabled MDAO optimizer [9] is that you need around 10 iterations per variable to get convergence. Figure 15 shows two sample plots of the first 10 solutions to get an idea about the level of correspondence and the variation.

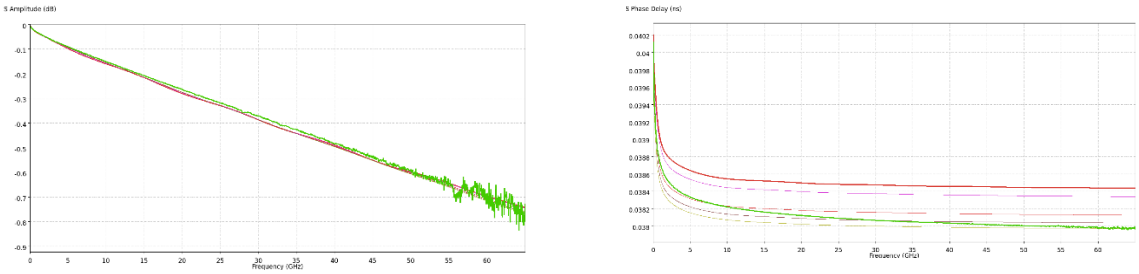

Figure 15 Fit of insertion loss (left) and phase delay (right) of the proposed solutions for the first 10 iterations. The starting point is shown in red and the measurement in green.

The optimization quickly found a good solution for insertion loss magnitude, while it is clear that the phase delay converges more slowly, or said another way, the phase delay is the most sensitive parameter here. Through the material identification process, we ended up with the following AF properties extracted from the measurement-based model, which are compared to our initial AD values:

	$Dk_{avg,\ pp}$	$Dk_{avg,\ core}$	r_{outer}	r_{inner}
As-Designed	2.94	3.11	0.3	0.069
As-Fabricated	3.29	3.038	0.182	0.148

Figure 16 Summary of As-Designed vs As-Fabricated material properties

Especially from the surface roughness values, it is clear why the AD setup might underestimate the loss for the stripline layers if we used just quoted surface roughness data. In addition, a note should be made regarding the 10% higher prepreg dielectric constant compared to the starting

point & core values. This comes back to the uncertainty regarding controlled impedance on outer layers – there is a large uncertainty in the solder mask coverage, the equivalent height of the solder mask and outer layer plating thickness influence, these will be discussed more in the next section. In hindsight we could have made core and prepreg Dk_{avg} identical and simply tuned the effective solder mask height and dielectric constant, but again, we must consider our objective which was to match the terminal behavior – in modeling as with many other things there are many ways to meet the modeling end goal.

With the material identified we tested our updated digital twin on several structures. Both the structures used for the material fit (2" and 8" transmission lines both microstrip and strip lines) as well as Beatty class structures and several others were used. Below shows two examples with both the Hausdorff metrics indicated (see refs 6,7 & 8 in [1]) and the TDR results. The closer the Hausdorff numbers are to 100 the better the match between the measured and simulated datasets. It has been suggested in ref 6 above that a Hausdorff number > 90 constitutes acceptable correspondence. We found all Hausdorff metrics for the structures examined to be 88 or higher in the range from 0-50GHz. The TDR results provide additional insight into the level of correspondence between the simulated and measured datasets.

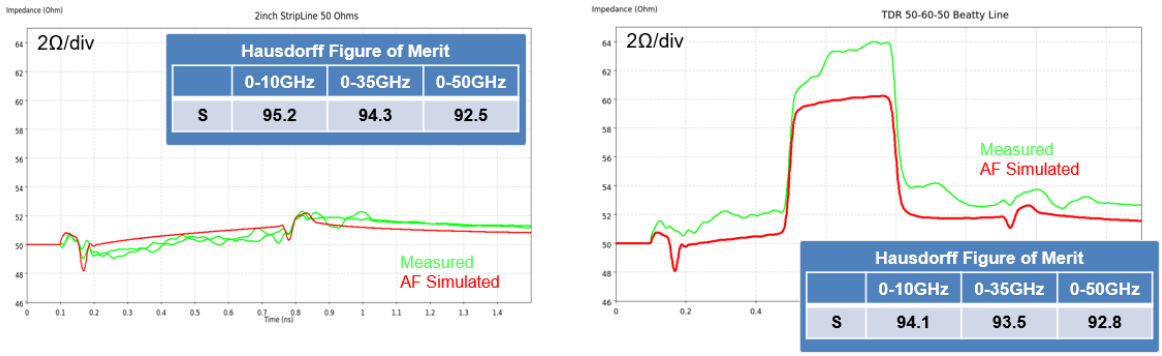

Figure 17 Correspondence between simulation and measurement with identified materials. 2" stripline (left) and 50-60ΩBeatty class structure (right). Both includes the connectors – i.e. full path simulation.

We see that for the 2" stripline model the TDR is within 0.5Ω from the measurement while for the Beatty class structure shows much more variation – around 1Ω difference in the 50Ω sections and up to 4Ω difference in the 60Ω section. It's important to note that the digital twin exhibits behavior that we would expect for a perfectly uniform transmission lines while the jumps in the measured TDR might at first seem surprising, with that, we now come full circle back to the manufacturing tolerances, material variation and the overall macroscopic SI aspects.

Manufacturing Variation

To further highlight the effects of manufacturing variation introduced at the end of the last section we shall explore the launch area around the connector. In the description of the test vehicle, we showed the cross sectional data used to update our simulation model, had we done cross section along a trace as well we would see the varying dielectric environment (thickness) and shape of the transmission line, These changes will of course cause a changes in the local impedance along the line as shown in Figure 18. The picture shows the TDR of nominally identical launch structures and lead-in traces to the test structures. The connector launch (the first two time divisions) shows some impedance variation but is better controlled than the traces which are within ±2Ω. Such variation of trace impedance is actually considered to be *tight control* as most designs today are manufactured with ±10% impedance tolerance which translates into typical impedance control of ±5Ω. In other words, you can expect a potentially large variation of a measured TDR versus a

digital twin model. Even if you are on average right, a TDR along an AF trace that is supposed to be uniform will vary along the length due to pressing thickness, Dk, etching variation etc.

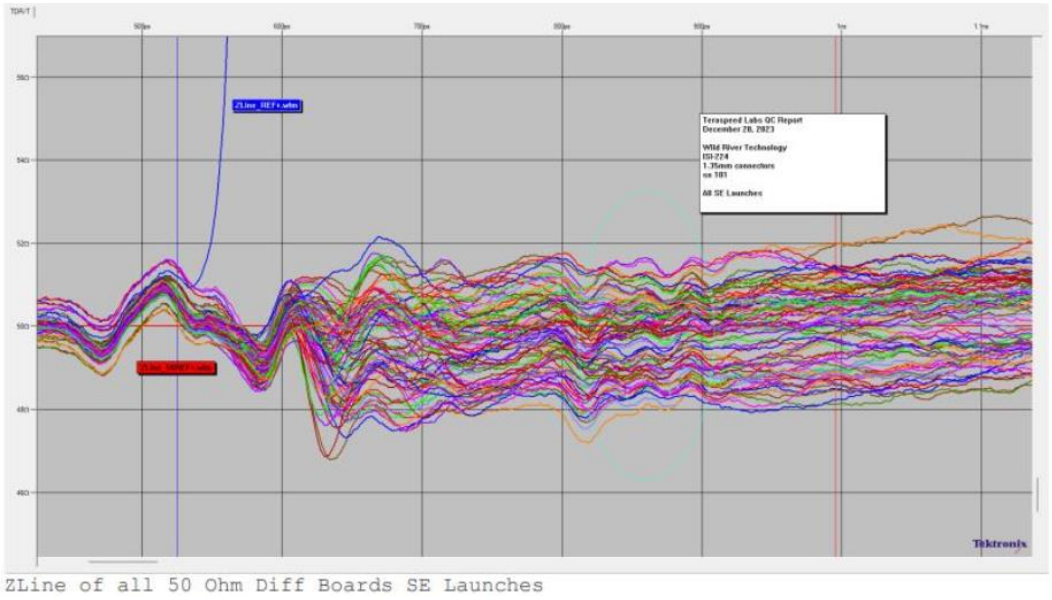

Figure 18 Variation in the measured impedance of the same line across the board and on different boards.

The variation in the PCB manufacturing process and in the materials themselves, coupled with the fact that the material identification is non-unique, will make identification of the anisotropic properties more difficult than we initially expected.

Anisotropic Dk

Although we modeled the PCB materials above using a bulk Dk, we know that actual PCB material is anisotropic due to the glass-weave / resin combination. Generally, anisotropy is modeled by a second-rank tensor (3x3 matrix), but a first order (uniaxial) model of the dielectric can be used which is simple a 3x3 matrix containing only diagonal elements. In the uniaxial model the in-plane Dk are the first two elements, and the Dk in the out of plane direction is the lower right element. This is adopted in part from the notation in [12].

$$\boldsymbol{Dk} = \begin{bmatrix} Dk_{=} & 0 & 0 \\ 0 & Dk_{=} & 0 \\ 0 & 0 & Dk_{\perp} \end{bmatrix}$$

The components are illustrated below

Figure 19 Dielectric material with indication of in-plane and out-of-plane Dk values

A simple figure of merit using the terminology from [13] defines the level of anisotropy as Λ with Λ defining the percentage of anisotropy with numbers ranging from 0 (e.g. for purely homogeneous dielectrics) and upwards, 12% being a typical maximum that might be encountered:

$$Dk_{=} = (1 + \Lambda/100)\mathrm{Dk}_{\perp}$$

This figure of merit is basically a measure of how much higher the in-plane Dk is relative to the out-of-plane Dk. Typical values of Λ in PCB materials are 5-20, i.e. $Dk_{=}$ is higher than $Dk_{\perp}$ by up to around 20%. This is important to know because anisotropy causes changed impedances, propagation delays, and crosstalk relative to the isotropic case [14]. Also because a via has a larger portion of energy in the out-of-plane direction, if we use typical datasheet values of Dk or use a bulk Dk as identified in above, we will end up predicting that via structures in the board are more inductive than what is manufactured. Also the trace impedance can be slightly off as we will see that in one of the following examples.

In discussing anisotropy, it is important to keep in mind that the SI metrics we explore are sensitive not only to the level of anisotropy but also small variations in the isotropic Dk, variations from manufacturing tolerance and variation in Dk of prepreg and core. Trying to identify the anisotropy in the laminate system it is important to explore whether the difference we see could also be caused by other factors, otherwise it could lead to wrong conclusions, thus attention must be given to defining suitable test structures and metrics with enough sensitivity to separate the relevant variables. Even then, we have found that separating the impact from inhomogeneous material properties, anisotropic material properties, and manufacturing variation in the AF structures can be very challenging and may introduce artifacts. In the following we explore three structures as candidates to separate the isotropic vs anisotropic Dk effects.

A Thru Via

The first example we will look at is a through via. The overall structure contains 3 through vias, 2 at the connector sites and one in the middle and half the trace routing in top side of the board, the other part on the bottom side. This structure is shown in Figure 20. The structure is from the predecessor of the present test vehicle.

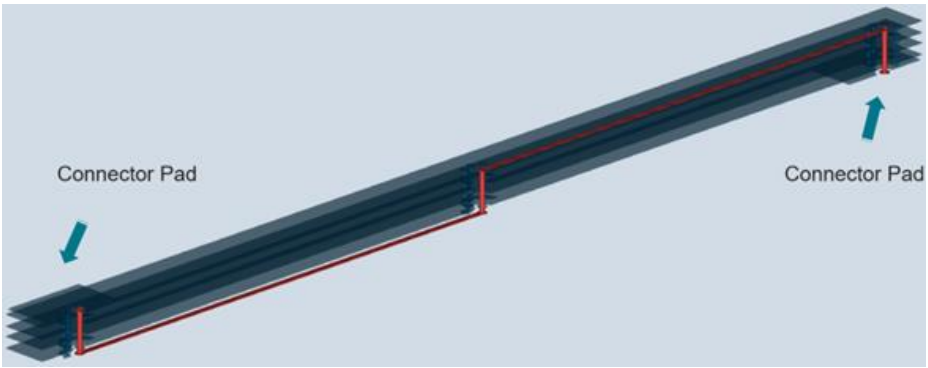

Figure 20 A complete channel with a through signal via in the middle.

Using nominal values for the features and isotropic Dk, this channel was simulated and the TDR response from one end displayed. We then examined the setup in two scenarios. One where we increased the bulk Dk by 10% and 20% over the nominal isotropic Dk and one where we increased the level of anisotropy to Λ=10 and Λ=20 while keeping the $Dk_{\perp}$ identical to the original bulk Dk. The results are shown in Figure 21.

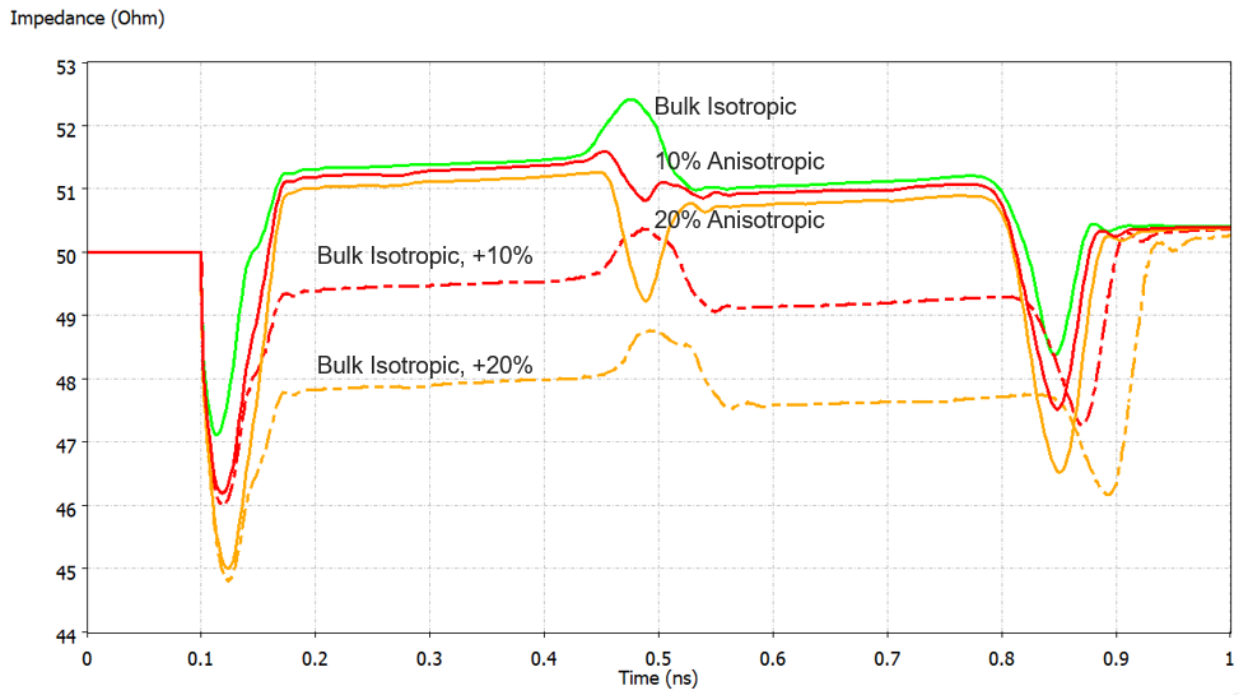

Figure 21 The simulated impedance of the microstrip traces and the through via with nominal conditions and then with a 10% and 20% increase of the isotropic and anisotropic Dk values

What did we expect to see? Well, scaling Dk by a given factor will modify the impedance by 1/sqrt($Dk_{multiplier}$). This implies that if we scale the bulk Dk by a factor of 1.1 (10% increase) we should see impedance reduce by close to 5% for both the via and trace and for a 20% increase we should expect to see a reduction by 9% and this is roughly what we see in above. For the anisotropic case the picture changes slightly because here we are only scaling Dk in the in-plane direction and thus dependent on the field distribution around a given structure the impedance scaling will vary. For instance, if we assumed that the trace fields were only in the out-of-plane direction, then the trace impedance would not change with any Λ. Similarly, if we assumed that the field in the via was purely in the in-plane direction then we should expect to see a 9% change of the via impedance for Λ=20. However, this is not exactly what we see because the field distribution is a combination of contributions from the in-plane and out-of-plane components. Thus, in the particular case examined the trace impedance changed moderately by less than 1Ω for Λ=20 while the via impedance was reduced by 6%. This suggests that a through via might be a good candidate to extract anisotropic material properties separate from the isotropic material properties. This is reasonable as there are considerable in-plane electric fields between the via barrel and the clearance hole planes, as shown in Figure 22.

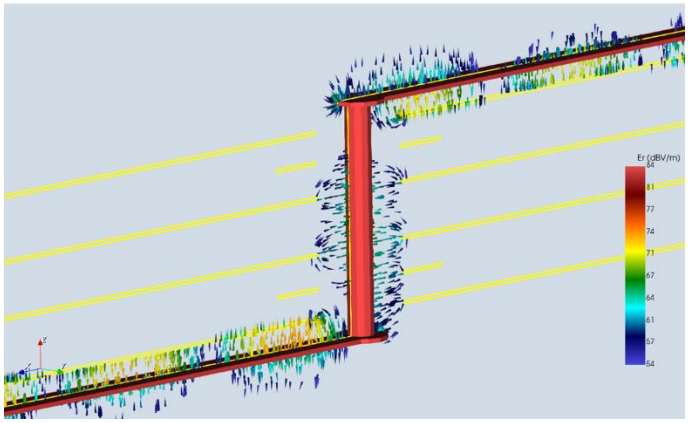

Figure 22 Example of the simulated electric fields in the microstrip and via transition. Note the dominant horizontal electric fields in the via region and the Z electric fields in the microstrip region. Left (isotropic) and right (20% anisotropic) – both shown on the same scale with 30 dB dynamic range.

If we want more sensitivity to anisotropy, it can be achieved through using narrower traces or a more capacitively loaded via. However, the challenge with both options is that they simultaneously increase sensitivity to manufacturing variation.

A Via Stub Resonator

The second structure studied was a via stub that extends from the top layer to the bottom layer as just a through-hole stub. This is effectively a quarter-wave stub resonator [5] and the structure is shown in Figure 23.

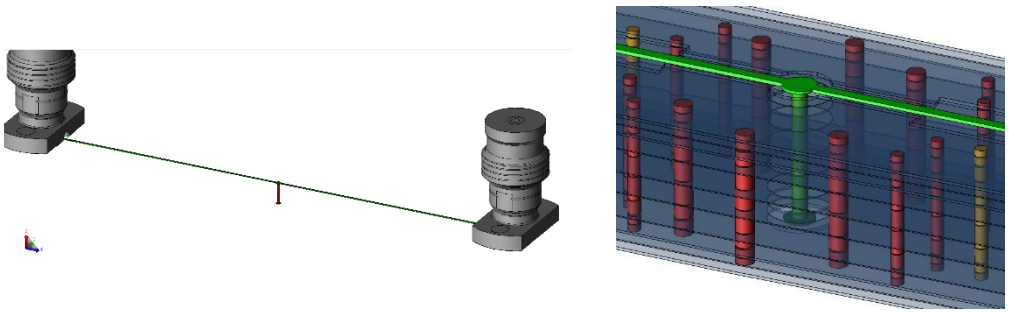

Figure 23 The via stub in the entire channel and its close-up show the cavity shorting vias as well.

The initial expectation was the resonant frequency of the via stub would be a sensitive measure of the Dk in the in-plane direction, $Dk_{=}$, but not the out-of-plane, $Dk_{\perp}$, direction.

A close-up of the measured insertion loss showing the resonant dip at the first quarter wave stub resonance of 13.5 GHz is shown in Figure 24. In addition to the measured insertion loss is the simulated insertion loss using nominal values for all the geometry features and using the bulk, isotropic Dk we identified earlier. We see a resonant frequency that is about 1 GHz lower compared to the of the measured value. When the anisotropic figure of merit, Λ, was increased, the in-plane Dk value increased, and the via stub resonant frequency decreased further, as expected. With each increase in the in-plane Dk by 5%, the resonant frequency decreased further by 1.5%.

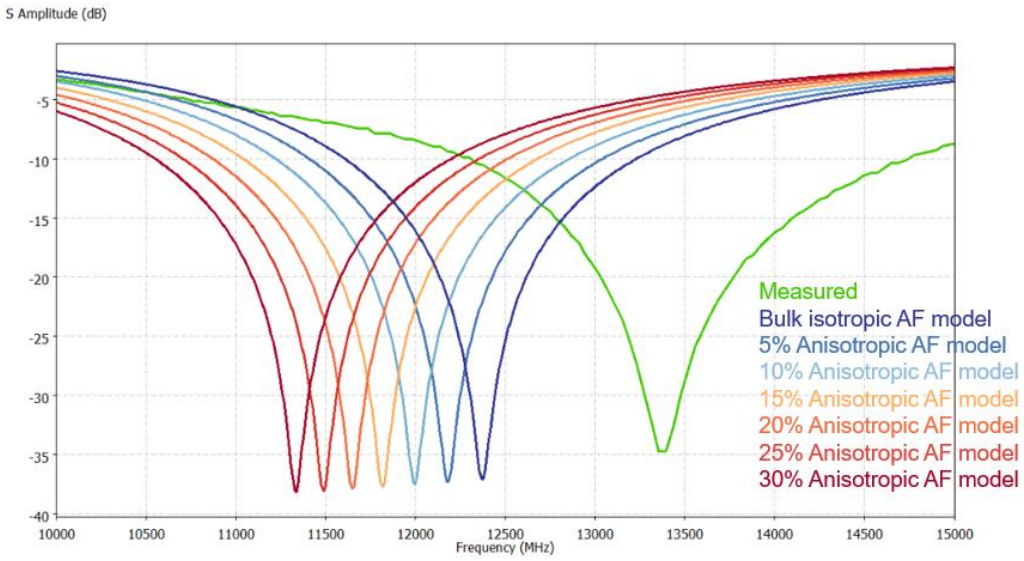

Figure 24 Insertion loss of the via stub was measured and simulated with the nominal features and an increasing level of anisotropy of the in-plane Dk.

As we would expect an increase in the isotropic bulk Dk alone also resulted in a similar shift in the resonant frequency. While the resonant frequency of the via stub is sensitive to the anisotropy term, it is equally sensitive to variation in the isotropic Dk term as we also learned from the previous section.

We know, to first order, that the resonant frequency of the via stub is related to the stub length and the Dk surrounding the via. However, the resonant frequency also depends on the capacitive loading from the capture pads and clearance holes through the planes. So instead of just simulating the stub resonator with the nominal geometry we included a sensitivity study where we changed the geometry according to the manufacturing tolerances. Amongst others we varied the clearance around the via / the antipad and pad on other layers by ±2mil from nominal as well as the drill offset, which can be as far as 3 mils off center. The changes we saw are summarized in below.

	Nominal	Antipad low bound	Antipad high bound	Drill offset	Pad on outer layers low bound	Pad on outer layers high bound
Resonance freq [GHz] (sim)	12.37	11.79	13.26	~12.3	12.75	11.97
Δ to nominal simulation case GHz	0	-0.58	0.89	-0.04 to -0.07	0.38	-0.4
Δ to nominal simulation case %	0	-4.7	7.2	-0.3 to -0.6	3.1	-3.2

Figure 25 Simulation sensitivity study of anisotropic resonator considering manufacturing tolerances

As is evident, the manufacturing tolerances, in some cases, produced far more variation on the resonant frequency than from an anisotropic material change. In fact, a 20% anisotropy only produced a 6% change in the resonance frequency while variation in antipad alone yields up to 7% change. Obviously, the fabricated geometry will vary along many dimensions and this serves to

mask the effects of anisotropy even further. In other words, with its present design, the anisotropic behavior is drowned out by manufacturing tolerances. The illustration in Figure 26 suggests why this is the case.

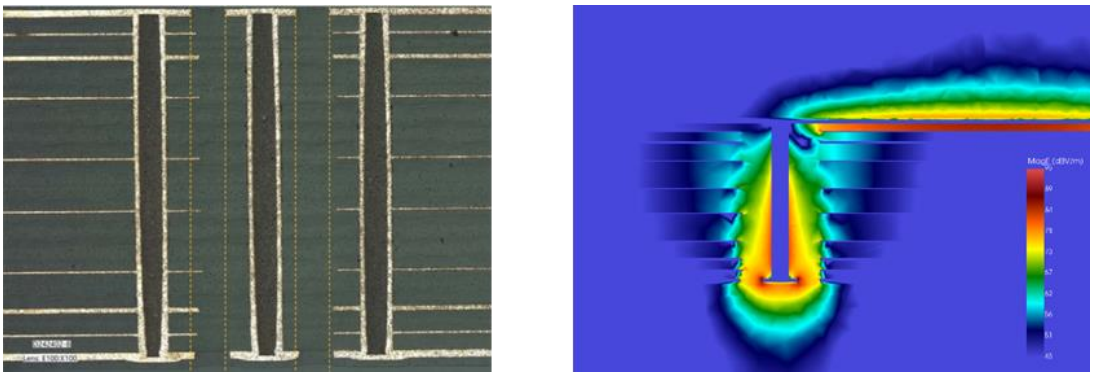

Figure 26 A cross-section of a via stub on the left shows the various capture pads and clearance holes. A field distribution plot on the right shows the fringe fields that contribute to the capacitive loading.

From the above picture, we see that the electrical field at resonance is highly impacted by the bottom pad and the surrounding metals. The exact antipad size, the registration of the layers and etching variation etc. are all contributing to a shift in the resonance. The cross-section around a via structure serves as a reminder that manufacturing-related tolerances should be considered in the design of test structures to ensure sufficient robustness of the structure.

This exercise points out that the via stub is not a good candidate for anisotropic materials identification in its present form, a redesign would be required, and outer layers are likely problematic to use for this kind of structure for similar reasons that it is difficult to control the impedance for microstrip lines.

Far End Crosstalk

The structure we found gave the largest *visual* sensitivity to anisotropy was the far-end coupling between two transmission lines. A simple way of thinking about the far-end crosstalk is that it occurs because of a difference in the propagation speed of the differential and common modes. It is also very sensitive to the fringe electric fields between the two lines, which are dominated by the in-plane Dk, that is, the anisotropic behavior. However, as before, the far end coupling is also sensitive to variation in the overall geometry and material mismatch – for instance variation in the coupling between the traces arise as a consequence of the inhomogeneous Dk mismatch between core and prepreg layers, trace width / etching and final pressed thickness. In addition, the material that actually exists between the traces is not the prepreg per se, but the resin flowing in between the gaps. Most resins used in PCBs, are not in themselves anisotropic so it is only the anisotropy of the material above and below the traces that matter, not the material immediately in between (you may refer back to Figure 12) so again we have some geometry dependence of the actual field distribution.

With this in mind we examined a pair of differential stripline traces on the CMP-70 platform. Figure 27 shows the measured S41, far-end crosstalk, and the simulated S41 using nominal values and the isotropic bulk Dk value we identified earlier (ISOMID). In this simulation, the Dk is not homogenous rather the Dk for core and prepreg layers are as established in as-fabricated values of Figure 16. The simulated S41 is generally much lower than the measured S41 over the entire frequency range. In simulation we had good correspondence with both differential insertion loss

with approximately 0.2dB difference between measured and simulated results and differential phase delay (overall Hausdorff metric from 0-50GHz was 89).

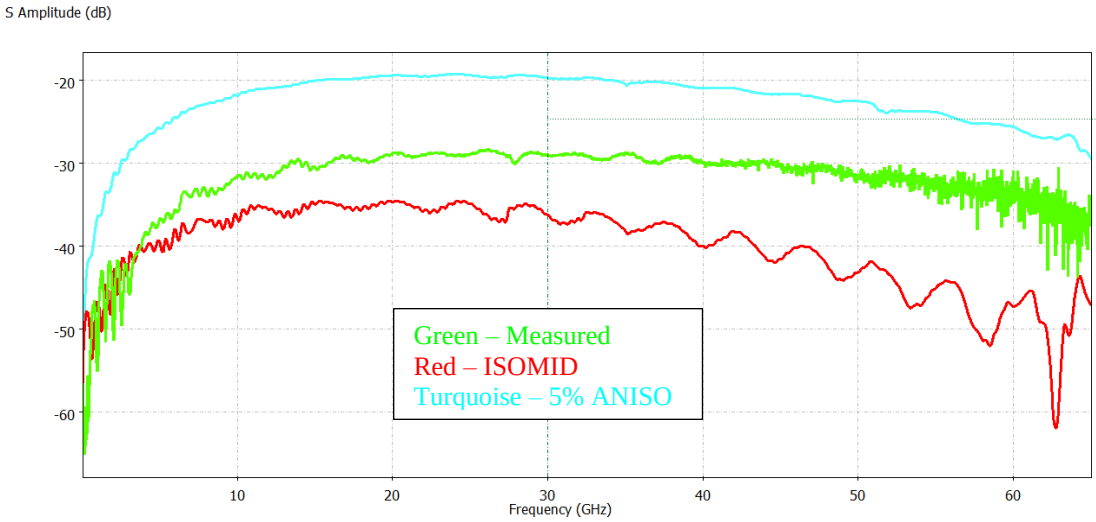

Figure 27 Measured (green) and simulated far end crosstalk in a 6" coupled stripline. The red curve is using an isotropic bulk Dk value and the turquoise is for Λ=5.

When the anisotropy figure of merit was increased from 0 to just 5%, the far-end crosstalk increased from about -35 dB at 20 GHz to -20 dB. This large change suggests a possible process to separate out the bulk isotropic Dk from the anisotropic Dk, but it also indicates that the solution is very sensitive to the material distribution. Interestingly, the Hausdorff number for the structure with Λ=5 decreased to 66, which indicates a large sensitivity to anisotropy in this structure. A more detailed study of the contributions from manufacturing tolerances is required before we can qualify this structure as useful for identifying anisotropy. Unfortunately, we did not have time to complete that study for this paper.

Overall, we believe, a potential solution for identifying anisotropic material properties of a laminate system might be to combine several structures into one model that is then simultaneously optimized. These structures could include:

1. A microstrip using the same prepreg layer as the stripline (sensitive to the Dk of the prepreg in the out-of-plane direction)
2. An uncoupled stripline (sensitive to the out-of-plane Dk of the core and prepreg)
3. The far-end crosstalk in a coupled microstrip (sensitive to the Dk of the solder mask and the anisotropy of the prepreg)
4. The far-end crosstalk in a coupled stripline (sensitive to the anisotropy of the core and the prepreg and the difference in Dk of the core and prepreg)

By optimizing these structures at the same time, the core and prepreg Dk might be extracted, and the anisotropic Dk figure of merit in both the core and prepreg might be obtained using the S41 term.

Finally, a through-via structure can be used to verify the final values of the nominal AF parameters and the Dk values. A key question for any such optimization approach is how you weight the different optimization metrics and what ranges are reasonable to use, this also remains to be

explored further, as is qualifying how many variables / degrees of freedom we actually need to identify what matters for our macrolevel SI.

Conclusion

In this paper, we have examined a few important aspects of channel design that impact design margin and channel requirements. Specifically, we have looked at some of the design aspects that cause a difference between the channel S-parameters from simulation based on what is available before fabrication (As Designed) to the measured fabricated PCB (As Fabricated). We saw a lot of difference in insertion loss that may results in a requirement to add more margin and/or use more complex equalization than is strictly necessary for design reliability.

By improving the simulation to measurement correspondence, we can gain more control of the system and come closer to realizing a digital twin that accurately predicts system behavior and allows us to explore the sensitivities of the key design metrics. The enabler for achieving better correspondence requires a shift towards using early-design-phase calibration PCBs that allow us to do the necessary material identification and process examinations. Such calibration PCBs can either be in-house or commercial solutions, the key is that the calibration PCB is done in the target laminate system using the same process settings that would be used for the full scale/mass production of the design. We need to move to a digital twin that is based on As Fabricated data.

With a calibration PCB, we can do material identification of the bulk isotropic dielectric constants, surface roughness models, and geometry aspects (e.g. solder mask height) from simple uncoupled transmission line structures. On the platform used we have seen very good correspondence in frequency domain using isotropic material properties on many of the structures but in time domain we see the anisotropic nature of the PCB material impact vertical structures such as vias. For this reason, we have examined a few structures to try to automatically identify anisotropy, but do not yet have a solution as the structures we examined showed large variation with several factors that cannot be distinguished from anisotropy.

Further work is required to identify structures that have the necessary sensitivity to anisotropy for a fully automated material identification procedure to be established.

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