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Conference

January 28–30, 2025

Santa Clara Convention Center

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January 29–30, 2025

Free signal integrity?

How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond

Eric Bogatin (University of Colorado)
Kristoffer Skytte (Cadence)

Alfred P. Neves (Wild River Technology), John Phillips, (Cadence), Frank Zavosh (Cadence)

SPEAKERS

Eric Bogatin

Professor, University of Colorado
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Eric Bogatin is a Professor at the University of Colorado, Boulder where he teaches undergraduate and graduate courses on signal integrity and system design. Additionally, he is the Dean of the Teledyne LeCroy Signal Integrity Academy, at www.beTheSignal.com and a Fellow with Teledyne LeCroy. He is also the technical editor of the Signal Integrity Journal

Kristoffer Skytte

Application Engineer Architect, Cadence
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Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. His recent efforts are on examining differences between measurement and simulation. He holds an M.Sc.EE. degree from the Technical University of Denmark.

SPEAKERS

John Phillips

Sr. Principal Application Engineer, Cadence

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John has 30+ years experience working on SI, PI, and EMC challenges at the chip, board, and system level in applications including high-end computing and mil-aero. He holds an MSc. from Bolton University, UK. His current interests are SI/PI co-simulation and modelling for high-speed interfaces.

Frank Zavosh

Solutions Architect, Cadence

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Frank received his PhD in Electrical Engineering from Arizona State University in 1995. He has 15+ years of experience as an RF/MW and antenna design engineer at various companies including Motorola and Philips Electronics. He worked as SI/PI/EMI Application Engineer at Cadence for 10 years. He is currently the Product Engineer for Cadence's Clarity full-wave FEM field solver.

Alfred P. Neves

Founder and Chief Technology Officer at Wild River Technology

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Al has 39 years of experience in the design and application development of semiconductor products, capital equipment design focused on jitter and signal integrity analysis and has successfully been involved with numerous business developments and startup activity for the last 17 years. Al focuses on measure-based model development, ultra-high signal integrity serial link characterization test fixtures, high-speed test fixture design, and platforms for material identification and measurement-simulation to 70GHz. He earned a B.S. in Applied Mathematics at the University of Massachusetts.

INTRODUCTION

- Free Signal Integrity?
- Typical sign off on As Designed information
- What difference can we expect between As Designed vs As Fabricated Hardware?
  - How much insertion loss margin are we leaving on the table?
  - Tolerances?
  - Anisotropy of PCB material gaining more focus

GOALS

- Examine difference between as designed and as fabricated - how much insertion loss margin is left on the table?
- Examine influence of anisotropy
- Perform material identification using AI
  - Isotropic vs anisotropic materials – bandwidth limits?
- Examine variation of electrical performance with design tolerances
- Suggest ways to improve digital twin

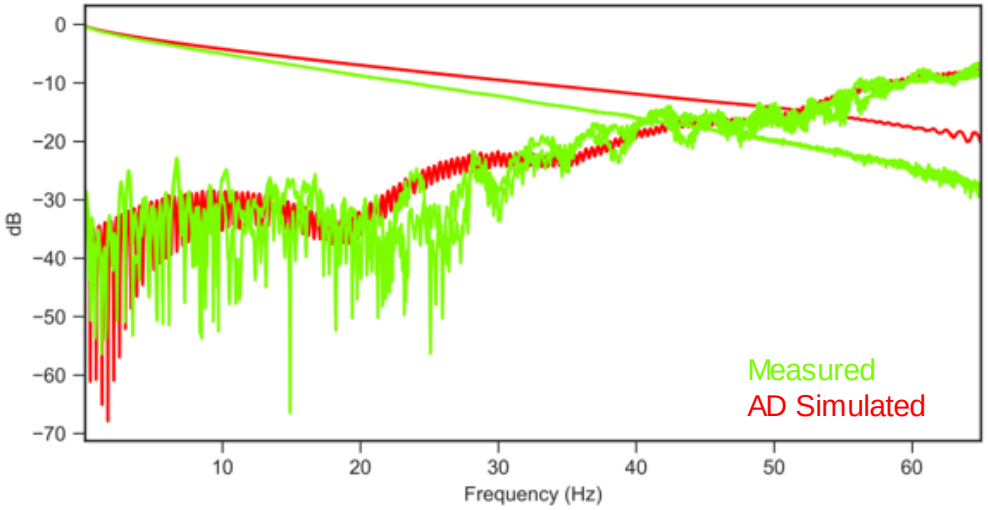
TERMINOLOGY

- As Designed (AD) – results from ECAD design database and vendor-supplied input prior to hardware becoming available – what is typically used for sign off
- As Fabricated (AF) – measured results from physical hardware, or simulation using x-section analysis, and fitted material parameters
- Digital Twin – model of the real-world hardware used in simulator environment
- Microscopic SI – SI of localized structures or of a specific channel
- Macroscopic SI – SI considering variation due to manufacturing, e.g. SI of single channel / channel to channel / variation across board / board to board / fabricator to fabricator

AS DESIGNED (simulated) VS AS FABRICATED (measured)

- Sample correlation for 70GHz Platform
- Simulation done based on best available information for sign-off in a typical design process
- Very good correlation on return loss
- Insertion loss suffers due to uncertainty mostly in surface roughness
- How much insertion loss margin are you willing to allocate to such gap in your system budget?

8" Stripline, Full Path

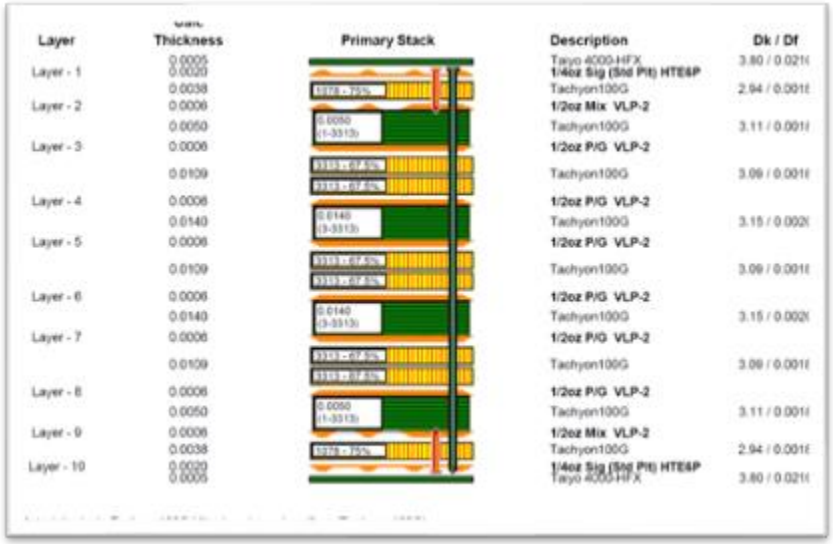


Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
S	62.4	61.8	63.3

Hausdorff = 0 (no correspondence)
Hausdorff = 100 (identical curves)

AS DESIGNED

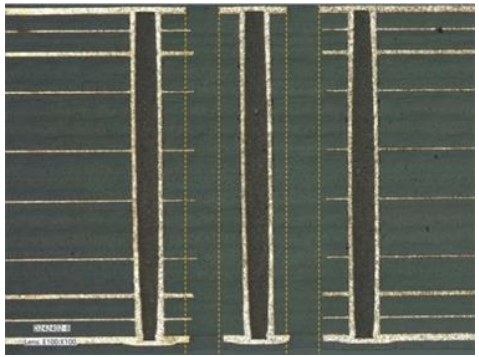
- Typical assumptions
  - Materials from datasheets or previous experience
  - ECAD layout database (nominal dimensions)
  - Stackup from PCB manufacturer
  - Simulation setup / boundaries*
  - Connector models etc

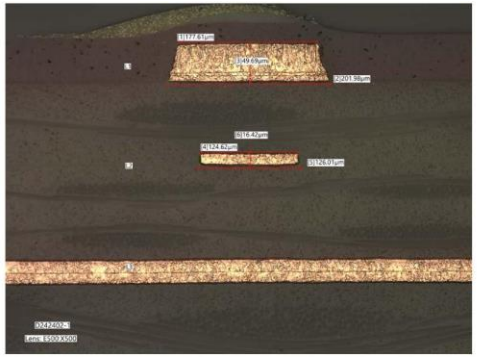


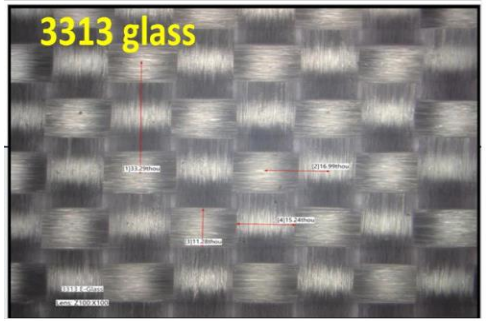
* K. Skytte, J. Phillips, S.-J. Kim, N. Trobough and A. P. Neves, The influence of EM field solver numerical solution space on measurement correlation to 50GHz and beyond, DesignCon, 2023.

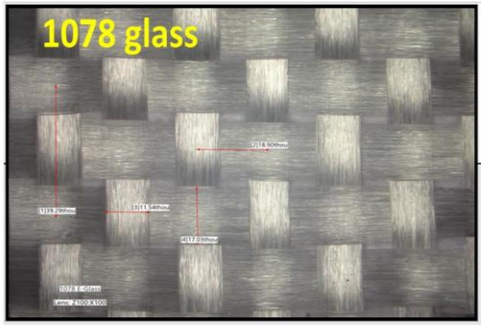
AS FABRICATED – PCB STACKUP VARIATION

- Uncertainties in geometry
  - Etching
  - Trace width and spacing
  - Layer registration
  - Layer thickness
- Uncertainties in material
  - Dk variation over panel
  - Resin variation
  - Material anisotropy / Weave parameters
- Uncertainties in manufacturing
  - Drill: wander / centering / backdrilling
  - Component variation e.g. pin centering
  - Variation between fabs!
  - Variation between batches
- The behavior of the PCB has a complex statistical variation





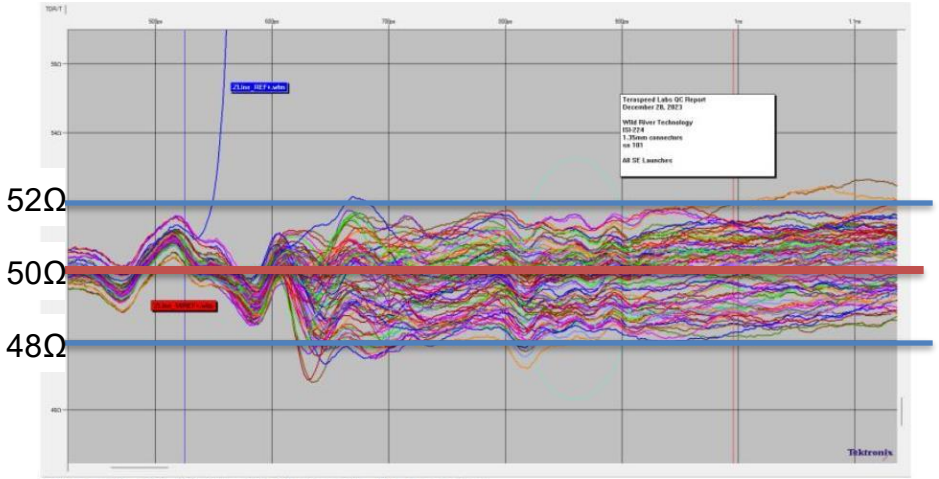




DIGITAL TWIN CHALLENGES

- It is unrealistic to assume what we simulate and what we fabricate are identical
- Digital Twin is challenged by 3 factors
  1. As Designed inputs different from as fabricated board
  2. Distribution of parameter variation not captured
  3. Many physical effects are not modeled
- Matching a specific channel we term **microscopic SI**, the variation in distribution of the channels is what we term **macroscopic SI**

Measured TDR of multiple launches on platform

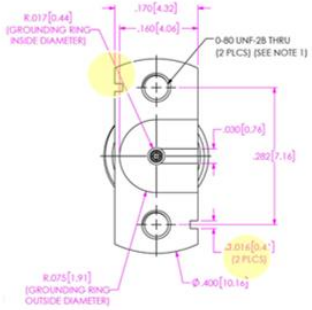


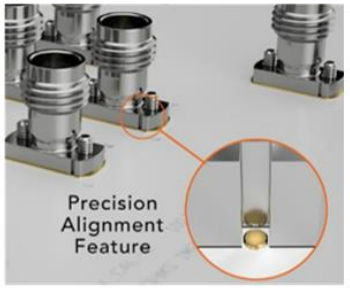
CMP70 – A 70GHZ TEST PLATFORM

- 70GHz Test Platform for 112G applications
- 10 layer Tachyon 100G laminate system
  - 1078 / 3313, low anisotropy
- Spread weave and angled (15°) routing
- HDI design (Microvias in launch region required)
- Finely tuned lauches
  - 1.85mm VLF connectors from Samtec
- Pristine reference measurements

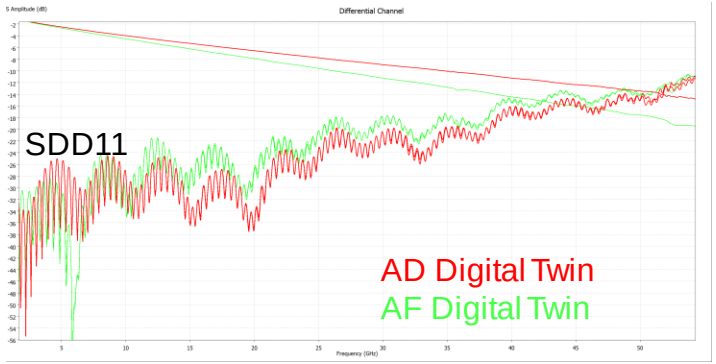
PLATFORM CONSIDERATIONS

- Platform concerns
  - Launch quality / assembly / repeatability
  - Single ended to differential transition
- Measurement best practices see previous paper*

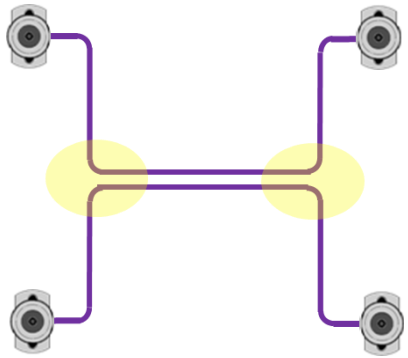




Pictures provided courtesy of Samtec
https://www.samtec.com/rf/connectors/185/



Launch assembly is imperative



* K. Skytte, J. Phillips, S.-J. Kim, N. Trobough and A. P. Neves, The influence of EM field solver numerical solution space on measurement correlation to 50GHz and beyond, DesignCon, 2023.

ANISOTROPY

- PCB is uniaxially anisotropic – characterized by two dielectric constants: in-plane $Dk_{=}$, and out-of-plane $Dk_{\perp}$

$$\boldsymbol{Dk} = \begin{bmatrix} Dk_{=} & 0 & 0 \\ 0 & Dk_{=} & 0 \\ 0 & 0 & Dk_{\perp} \end{bmatrix}$$

- Most quoted numbers / datasheets assumes just ***ONE*** Dk value. Could be either of above or a mix for an effective / bulk Dk value
- Why could this be important?
  - $Dk_{=}$ for PCBs are typically higher than $Dk_{\perp}$ (Λ = 5-20)
  - Vias have significant out-of plane electrical fields
  - Fabriacted via might end up being more capacitive than expected

Level of anisotropy can be expressed as*

$$\Lambda = \left[\frac{Dk_{=}}{Dk_{\perp}} - 1\right] * 100$$

* L. Simonovich, "A Heuristc Approach to Assess Anistropic Properties of Glass Reinforced PCB Substrates," in *Designcon 2023*, Santa Clara, 2023.

INFLUENCE OF ANISOTROPY – EXAMPLE

- A simple experiment with microstrip to microstrip transition (example with through vias from CMP50)

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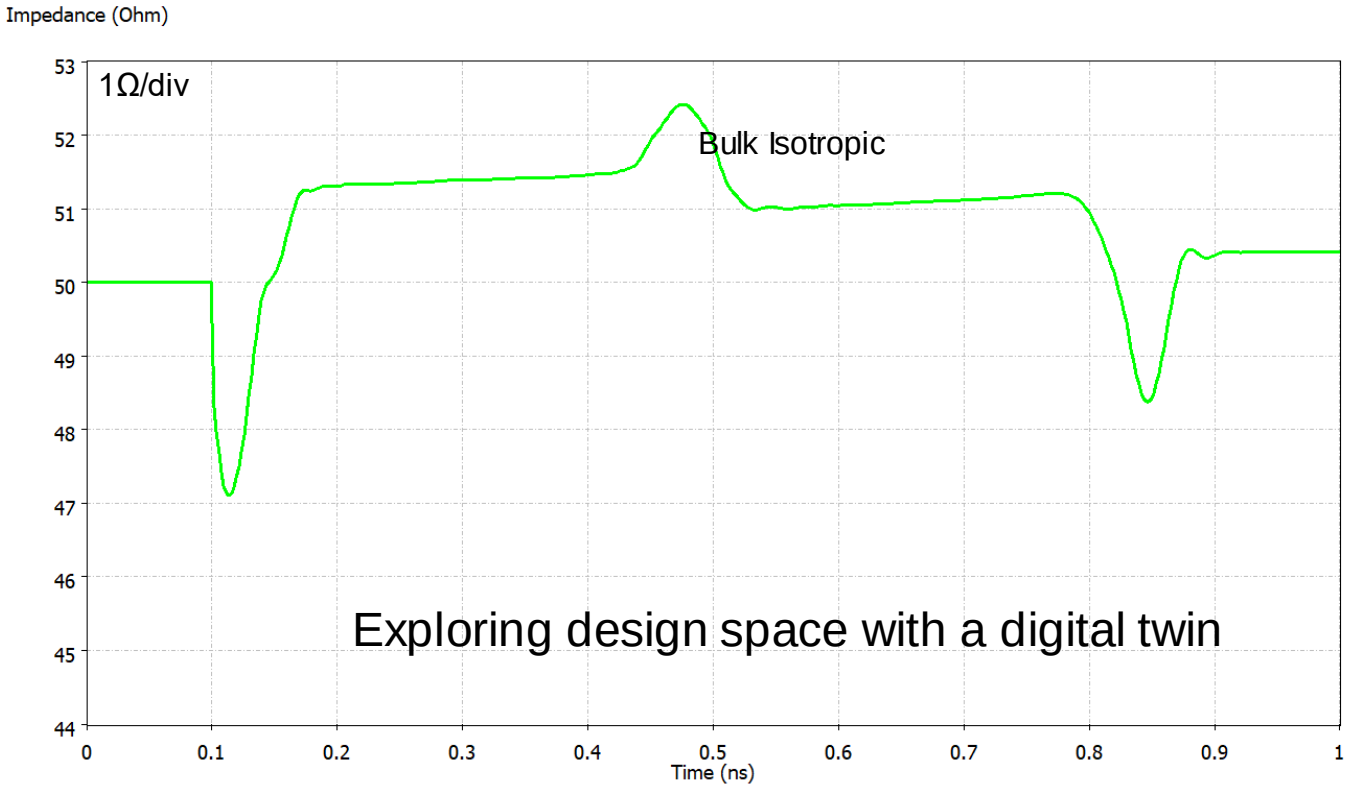
Bounding expectations

- From prortionality considerations we expect scaling Dk changes impedance as
  - $Z' = Z/\sqrt{D_{k,multiplier}}$
- If via fields were only in-plane and trace fields were only out-of-plane, anisotropy <20% would cause
  - Z trace change ≡ 0 %
  - Z via change < 9%

INFLUENCE OF ANISOTROPY – TDR



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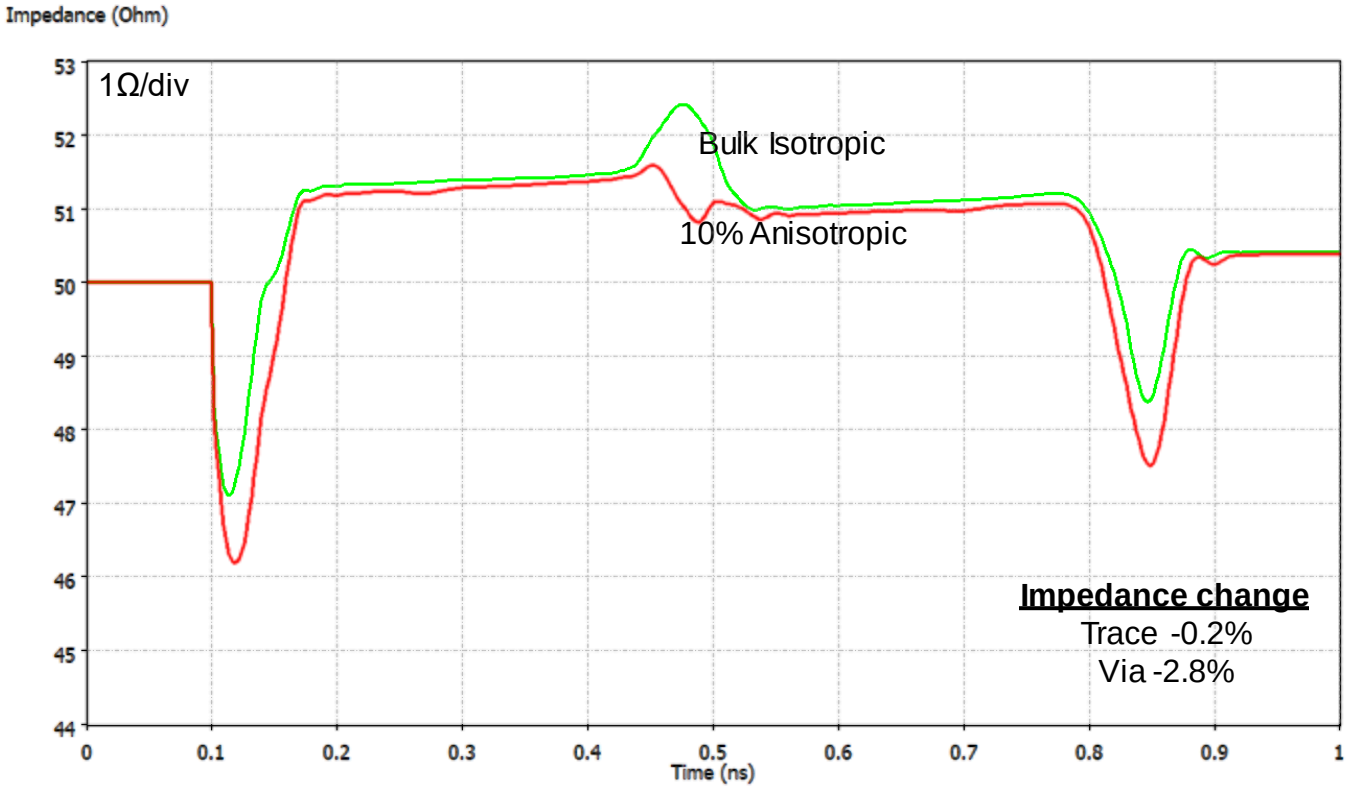

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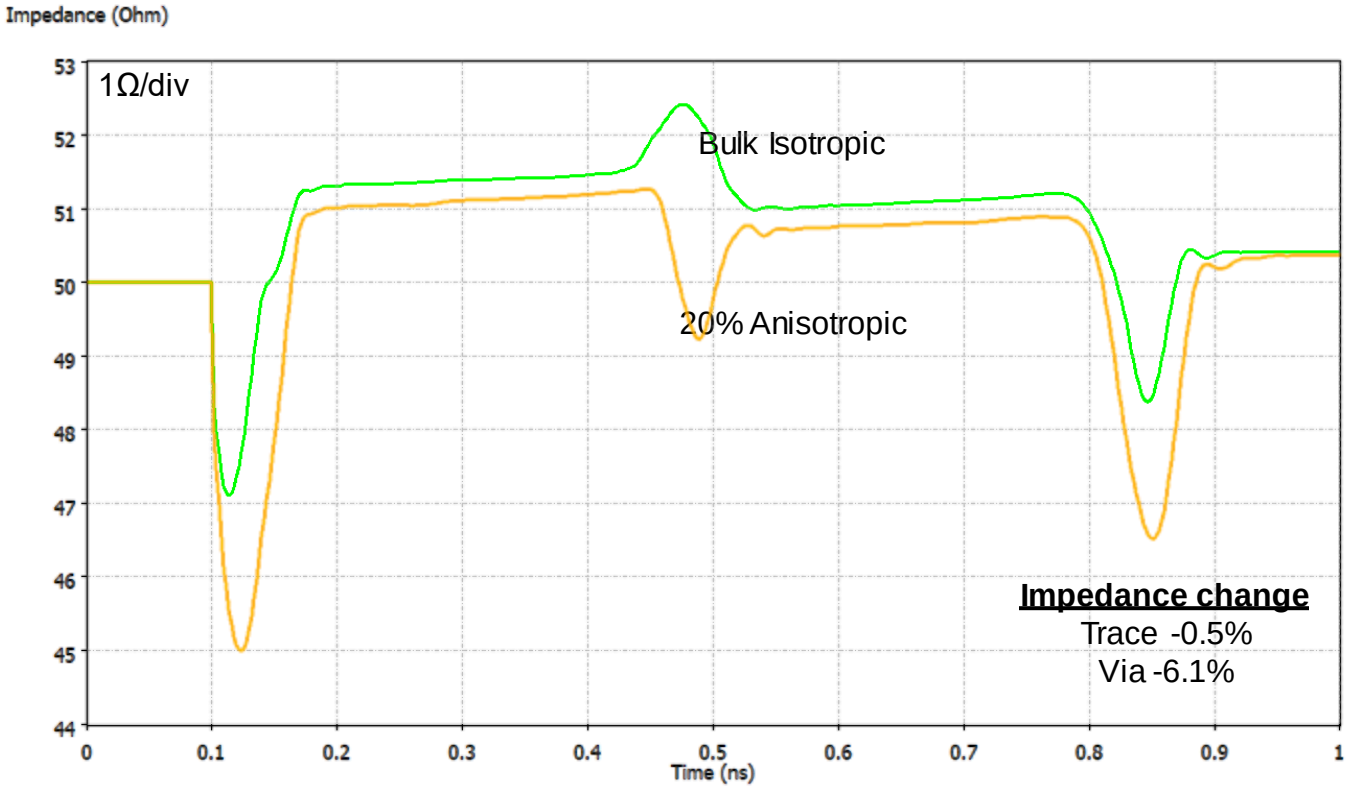

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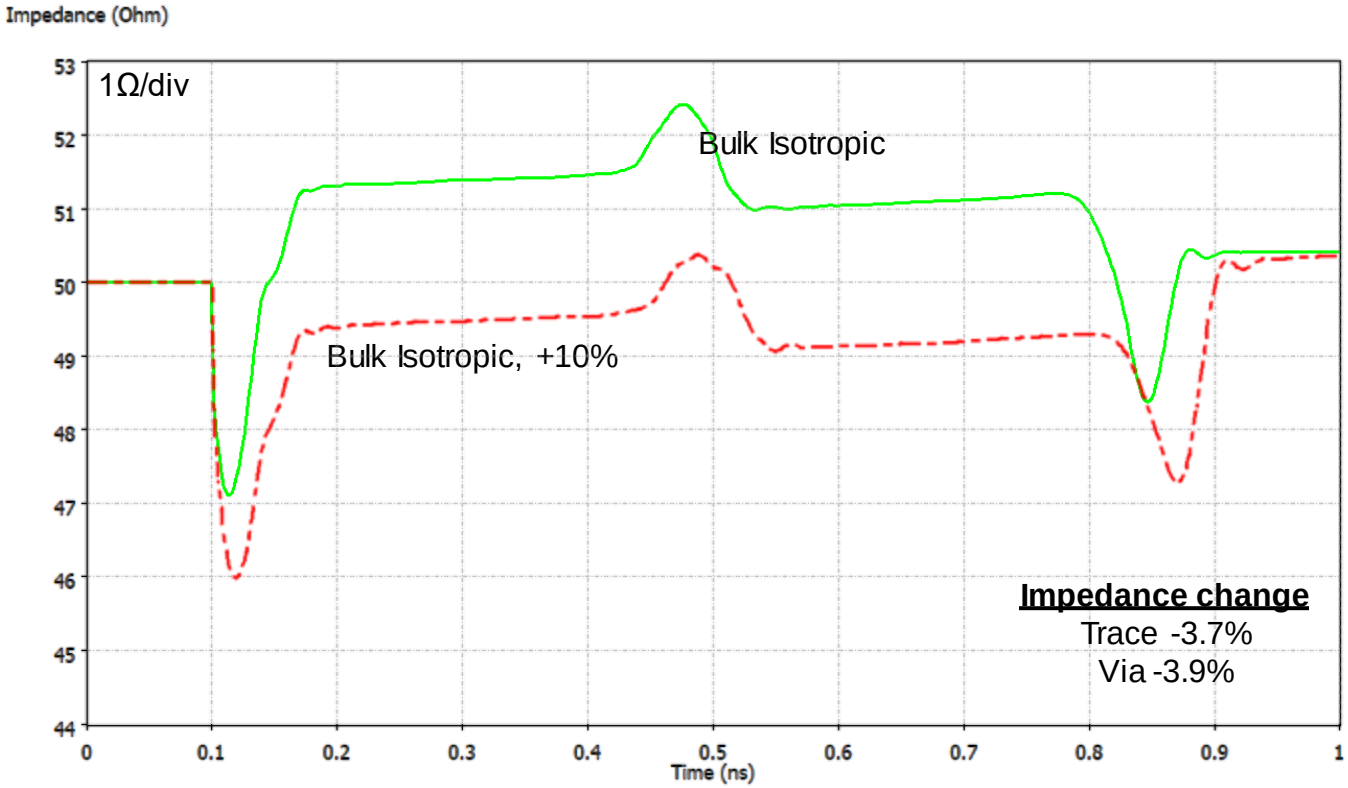
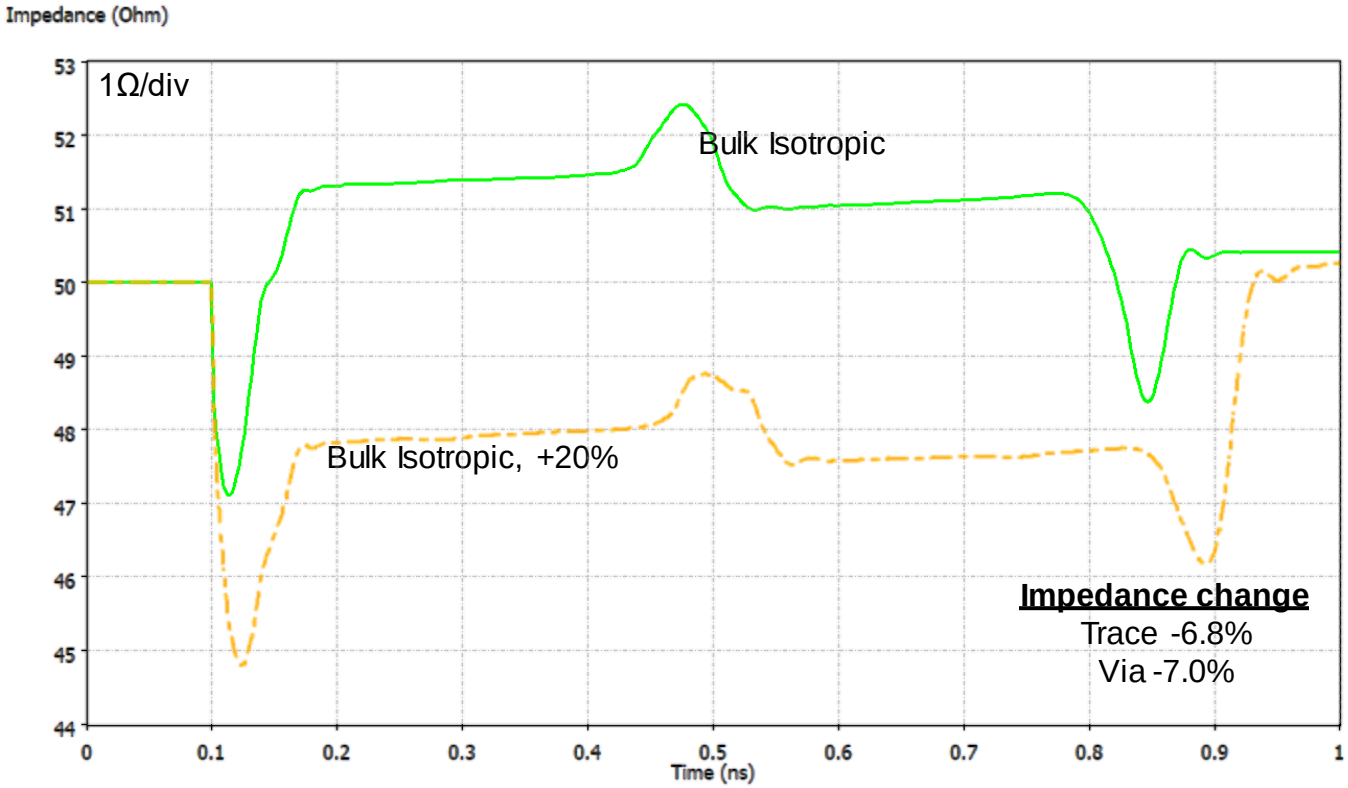
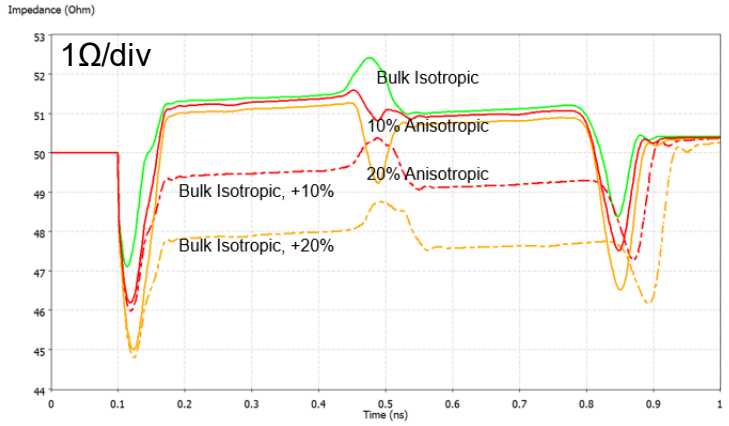


INFLUENCE OF ANISOTROPY – TDR



INFLUENCE OF ANISOTROPY – LEARNINGS

- Via impedance is more sensitive to anisotropic Dk values than trace impedance
- For the example with 20% anisotropy
  - Z trace change ~ 1%
  - Z via change ~ 7%
- Via fields and trace fields are not entirely in-plane and out-of-plane, respectively
- Actual change depends on the geometry configuration
- More sensitivity to anisotropy can be achieved
  - Narrower trace
  - More capacitively coupled via
  - Both options also increase sensitivity to manufacturing variation!

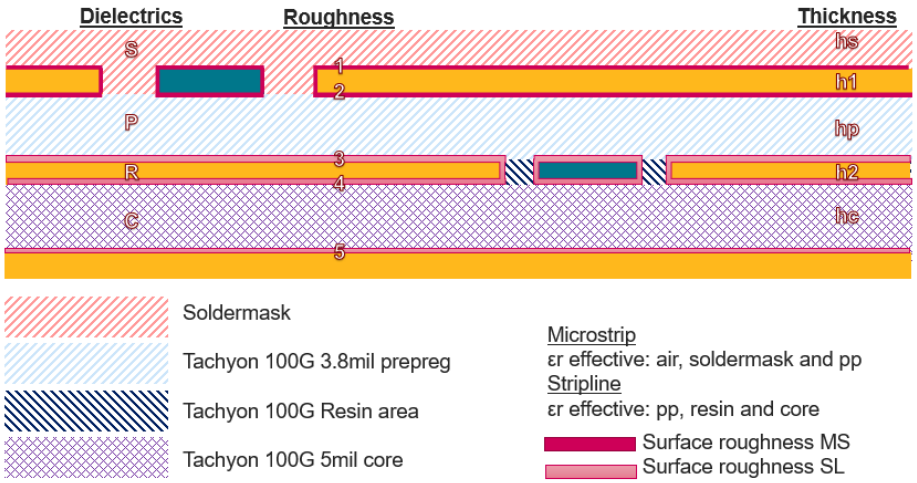


MATERIAL IDENTIFICATION PROCESS

- Material identification using single ended transmission line from measurement on the platform*
  - Using 2” and 8” microstrip and striplines
- Simultaneous identification of core, prepreg and surface roughness
  - Key consideration in optimization
    - Variables to be optimized / fixed / ignored or separated
    - Which optimization frequency range to use
    - What goal function to use
    - Trade off complexity for speed
    - Optimization engine selection – in our case an AI/ML based optimizer
- Verification using structures on the platform including the Beatty line standard

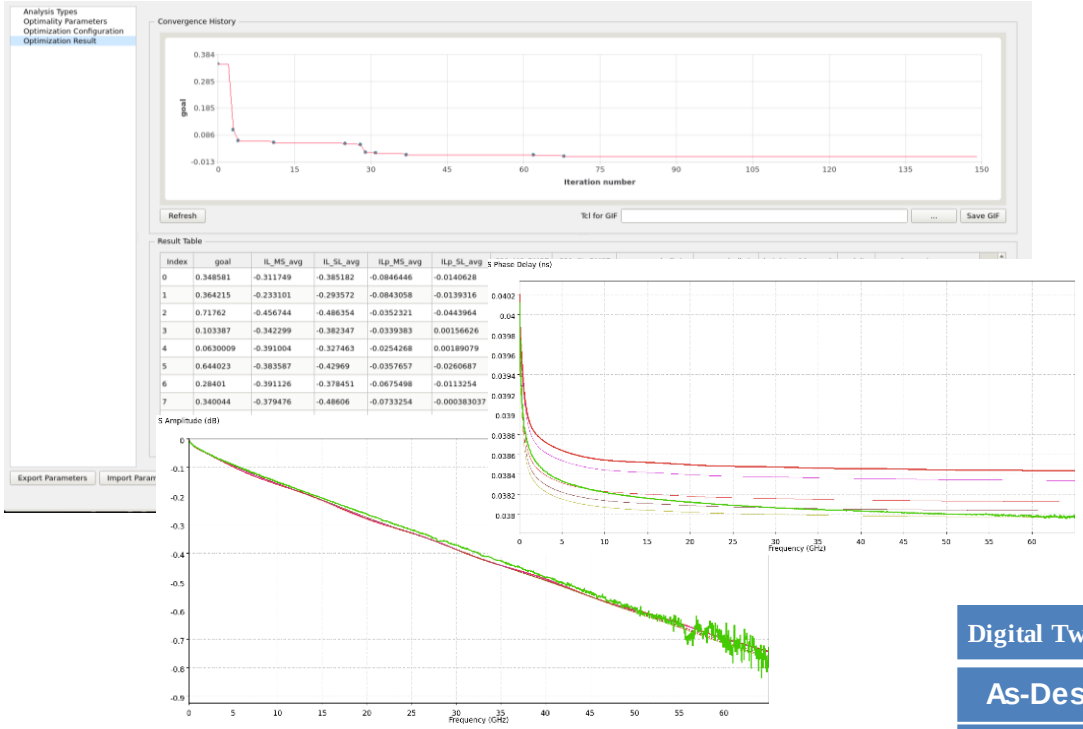
* K. Skytte, J. Phillips, S.-J. Kim, N. Trobough and A. P. Neves, The influence of EM field solver numerical solution space on measurement correlation to 50GHz and beyond, DesignCon, 2023.

MATERIAL FITTING ASSUMPTIONS



- Cross-section
  - Assumed height from x-section report (test strip)
  - Separated core and prepreg Dk
  - Different surface roughness for outer layers vs inner layers but not distinguishing between drum/rough sides
- Materials
  - Djordjevic Sakar 1GHz, Df from datasheet. Bulk isotropic
  - Huray Cannonball
- Optimize parameters to measured complex IL to 50GHz for both SL and MS simultaneously

OPTIMIZATION RESULTS

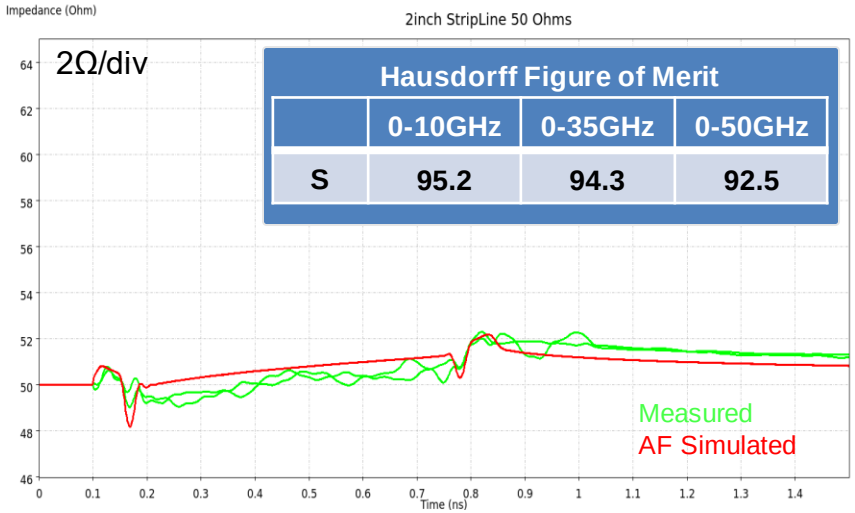


- Started from AD setup
- Phase delay is the last property to converge
  - choice of material models impacts transition behavior between “low” and “high” frequency -
- With current choice of setup, prepreg Dk is increased by 10% over datasheet values
  - Significant room for variation due to soldermask
  - Mapping to get good fit in specified optimization space is achievable in multiple ways

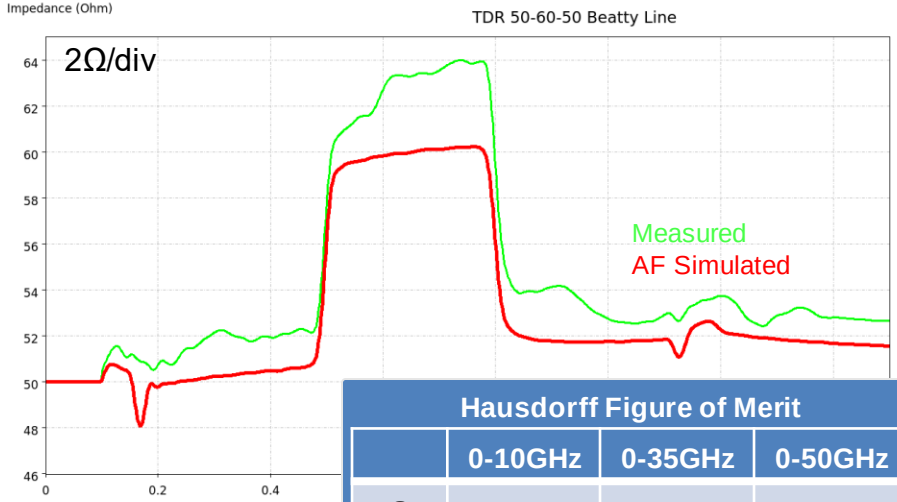
Digital Twin Setup	$Dk_{avg,\,pp}$	$Dk_{avg,\,core}$	r_{outer} [µm]	r_{inner} [µm]
As-Designed	2.94	3.11	0.3	0.069
As-Fabricated	3.29	3.038	0.182	0.148

MATERIAL FIT TO AS-FABRICATED

- Transmission lines used for material identification shows good correspondence in both frequency and time domain for full path structure
- Beatty line corresponds well in frequency but only reasonably well in time domain
  - Importance of tolerances and variation along length (macroscopic SI)



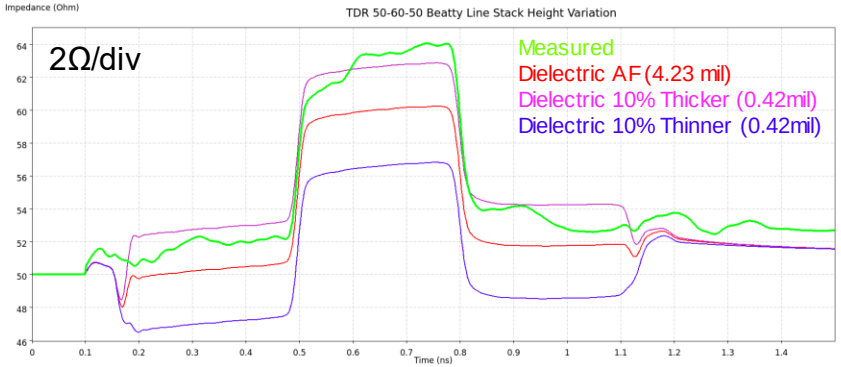
Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
S	95.2	94.3	92.5

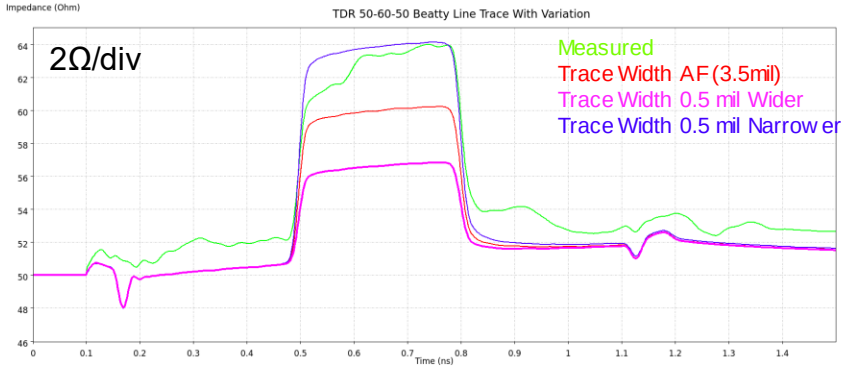


Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
S	94.1	93.5	92.8

MANUFACTURING VARIATION EXAMPLES (Macroscopic SI)

- Influence of manufacturing tolerances on Beatty line impedances, e.g.
  - pressed thickness (prepreg height)
  - changed only line width in 60Ω section
- Narrow traces are often used in break-out area



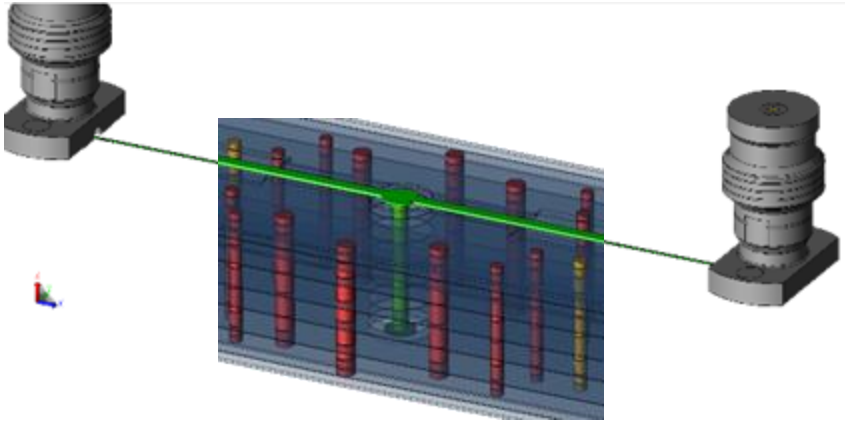


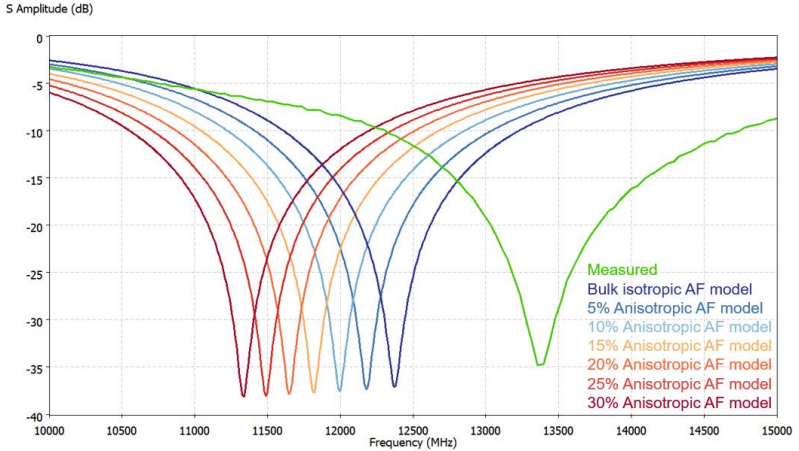
IDENTIFYING LEVEL OF ANISOTROPY

- How can anisotropy be identified and distinguished from manufacturing tolerances and other variations? Convolution of:
  - Anisotropy (% anisotropic)
  - Inhomogeneity (core, prepreg Dk)
  - Variation of h, w
  - non-uniqueness!
- Need to explore structures that exhibit a greater sensitivity to anisotropy
  - Through via (previous example of thru via TDR)
  - Anisotropic resonator
  - Coupled line
  - ….

ANISOTROPIC RESONATOR

- Via hanging off trace has been discussed as a potential way to identify anisotropy*





Resonance frequency from bulk isotropic material fit was off by 1 GHz from measured (12.4 vs 13.4GHz)

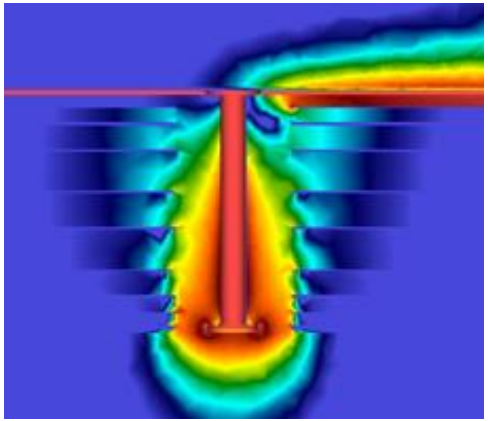
- Both isotropic Dk and anisotropic Dk pulls resonance further away roughly by 1.5% per 5% increase
- Macroscopic SI factors influence the resonant frequency

* S. McMorrow, E. Syre, . C. Nwachukwum and . D. Blackenship, "Anisotropic Design Considerations for 28GBs Via to stripline transitions," in *Designcon 2015*, Santa Clara, 2015.

VARIATION WITH GEOMETRY

- Why is the bulk Dk model so far off (1 GHz)?
  - A field plot shows significant field density around bottom pad and plane clearances – extra capacitive loading…
- We can explore sensitivity of the manufacturing variation using a digital twin
- With typical production tolerance on pad, clearance and drill we see more change with geometry than by Λ (only 0.2 GHz shift with 5% anisotropy)

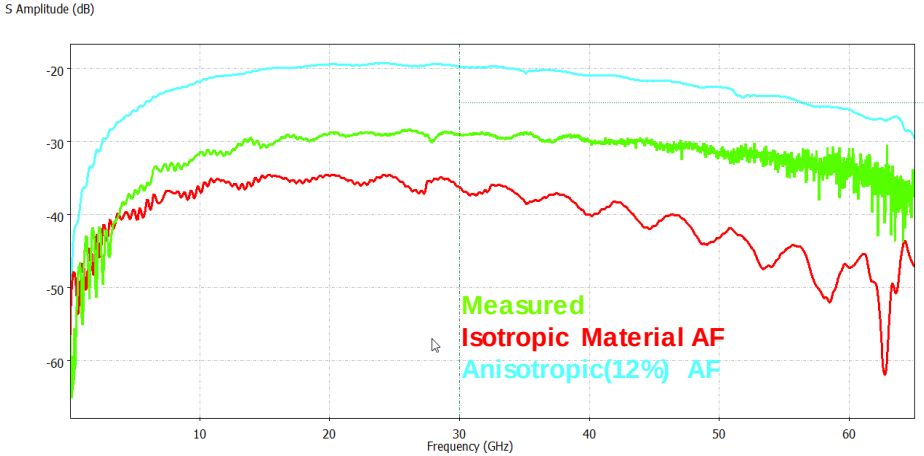
Electrical Field at resonance



	Nominal	Antipad low bound	Antipad high bound	Drill offset	Pad on outer layers low bound	Pad on outer layers high bound
Resonance freq[GHz] (sim)	12.37	11.79	13.26	~12.3	12.75	11.97
Δ to nominal simulation case GHz	0	-0.58	0.89	-0.04 to -0.07	0.38	-0.4
Δ to nominal simulation case %	0	-4.7	7.2	-0.3 to -0.6	3.1	-3.2

ANISTROPY AND FAR END CROSSTALK (S41)

- Anisotropy increases the in-plane capacitance – so increases crosstalk
  - Using only an isotropic material Dk underestimated the crosstalk
  - Also sensitive to inhomogeneous Dk and geometry
- Fruitful area for future exploration



Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
Isotropic (AF)	90.3	87.6	88.5
Anisotropic 12% (AF)	78.2	59.4	65.8

CONCLUSIONS

- Uncertainty in PCB fabrication process and material properties makes signing off on As-Designed PCB a risky affair
- Automatic material identification of bulk-isotropic properties using an AI enabled optimizer is feasible and gives good correspondence to measurement
- Further research is needed for anisotropic material identification that is decoupled from inhomogeneous materials and manufacturing tolerances
- Digital twin recommendations
  - Control insertion loss margin using early-design-phase calibration platform in the target laminate system
  - Need to extract relevant material properties from fabricated test platform
  - Explore sensitivity of metrics from each geometry and material term – we need macroscopic SI
  - Bound expectations and challenge your assumptions

Thank you!

QUESTIONS?

Kristoffer Skytte

Application Engineer Architect, Cadence

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