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DesignCon® 2026

WHERE THE CHIP MEETS THE BOARD

Conference
February 24–26, 2026
Santa Clara Convention Center

Expo
February 25–26, 2026

AI-Focused Success Vectors for Achieving Strong Simulation-to-Measurement Correlation

Alfred P. Neves (Wild River Technologies)

Kristoffer Skytte (Cadence),John Phillips (Cadence)

SPEAKERS

Alfred P. Neves

Founder and Chief Technology Officer at Wild River Technology
al@wildrivertech.com

Al has 39 years of experience in semiconductor product and capital equipment development, specializing in jitter and signal integrity. For 17 years he has supported business development and startups. His work focuses on measurement-based modeling, test fixtures, and measurement-to-simulation correlation to 70 GHz. He holds a B.S. in Applied Mathematics from the University of Massachusetts.

Kristoffer Skytte

Application Engineer Architect, Cadence
kskytte@cadence.com

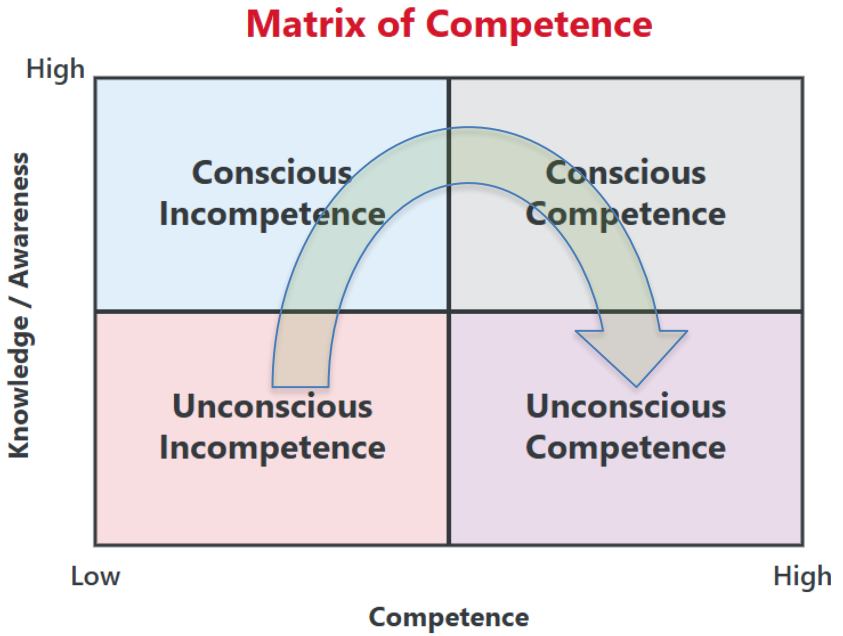
Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. One of his key interests is understanding discrepancies between measurement and simulation, and how our underlying assumptions influence what we observe. He holds an M.Sc.EE. degree from the Technical University of Denmark.

OUTLINE

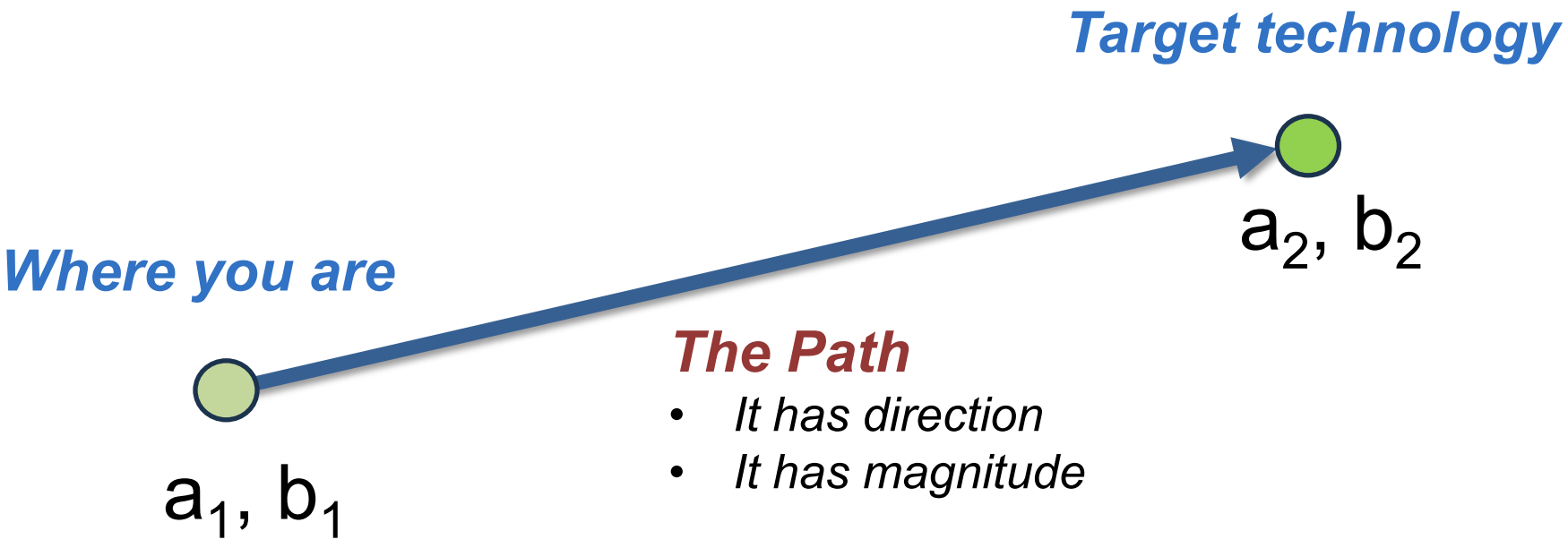
- This presentation explores **key considerations** and tradeoffs involved in **achieving** predictable **simulation-to-measurement** alignment versus technology goals in the Serial Link design space
- The experiment first establishes a logical starting point
- It demonstrates success vectors for a span of technology challenges
- We include some relevant background
- End goal is to better understand the problem of selecting a material ID strategy – **we start, we explore trajectories, we develop best practice endpoints… we vectorize**

What gets in the way of achieving Extreme SI?

- Leadership / Management / Organizational Strength
- Investment and capitalization in the right areas
- **Consistency of a path of constant SI improvement**
- **Developing engineering skillset both conscious and unconscious**
- **Know your vector – where you are, what your direction is, and where you are going, always migrating clockwise in the Matrix of Competency**



THE SIGNAL INTEGRITY VECTOR



The Path

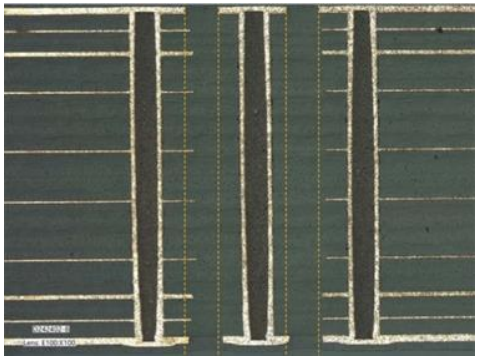
- *It has direction*
- *It has magnitude*

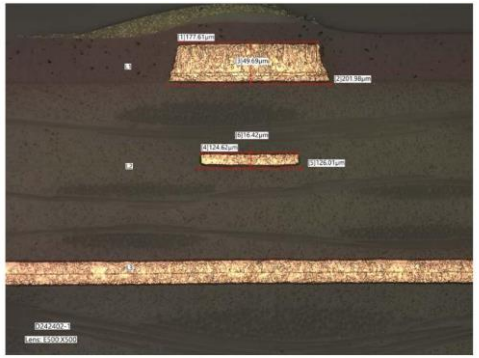
REVIEW

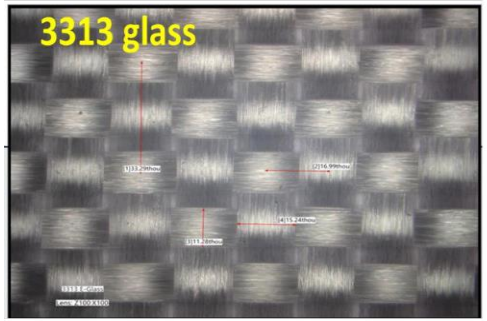
- Macro- versus Microscopic Signal Integrity
- The problem of measurement
- Full path simulation methodology
- EM boundaries
- Metrics of comparison

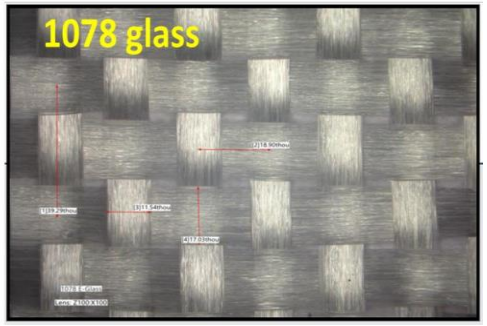
THE MICROSCOPIC VIEW OF SIGNAL INTEGRITY

- Understand what impacts specific structures
  - Uncertainties in geometry
  - Uncertainties in material
  - Uncertainties in manufacturing
- We can get cross section data, but typically only for one or two parts and not the entire board
- How to ensure design success across the board, across batches etc?

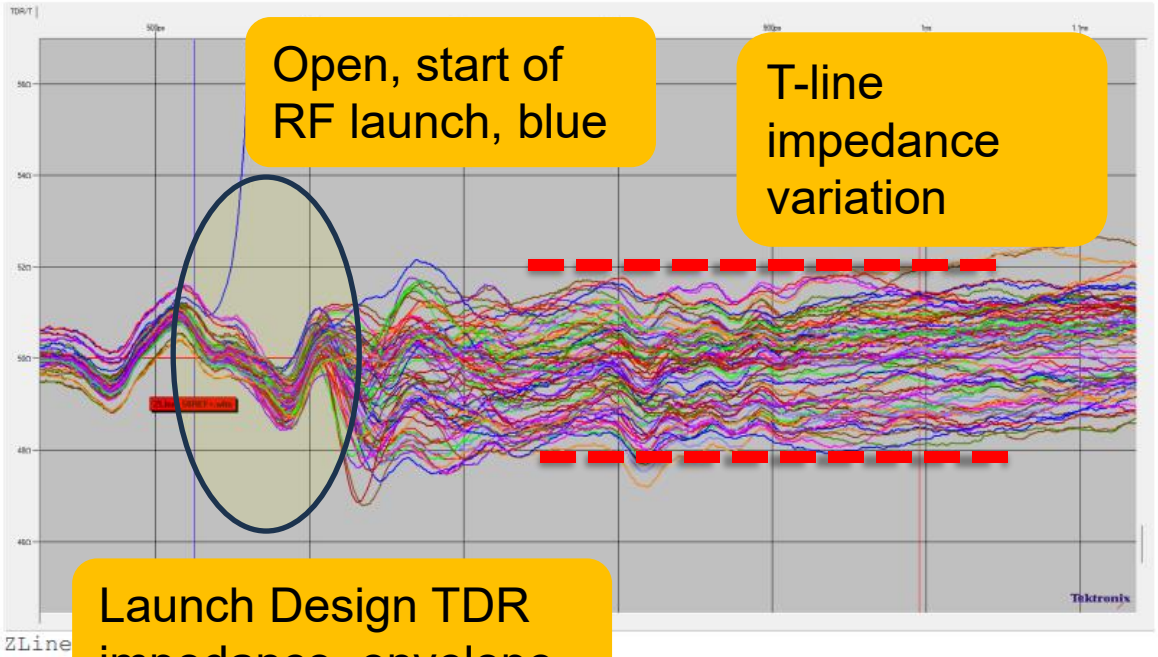




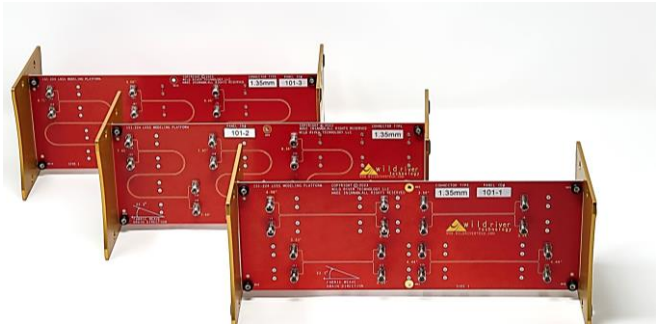




MACROSCOPIC SIGNAL INTEGRITY



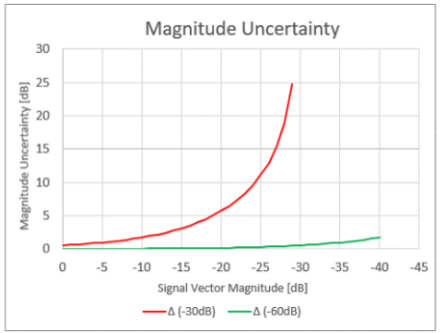
1.35mm 90GHz launch design better than +/- 1ohm, which is less than Tachyon100G material and fabrication etch weave TDR impedance spread.

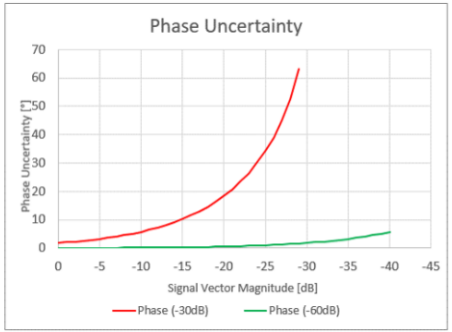


Skytte et al "Free signal integrity? How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond", DesignCon 2025

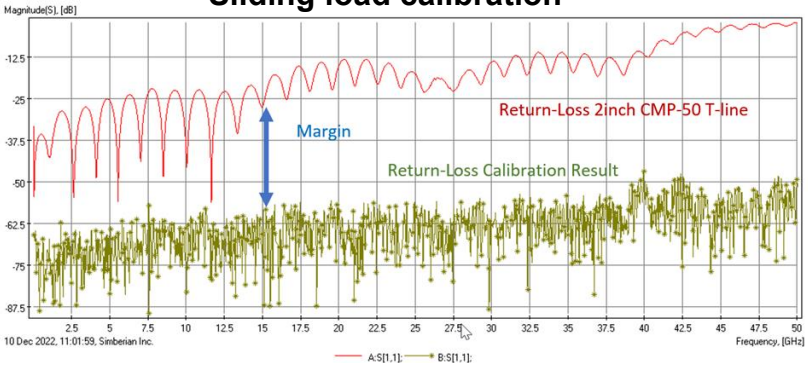
HOW GOOD ARE YOUR MEASUREMENTS?

- Return-loss calibration margin is essential for reducing uncertainty for both mag/phase
  - Mag/phase errors directly impact simulation to measurement correspondence
  - Inadequate margin impacts simulation to measurement vectorially, impact is asymptotically significant
  - ***Impact becomes more significant when return loss is low or your in ESI region!***

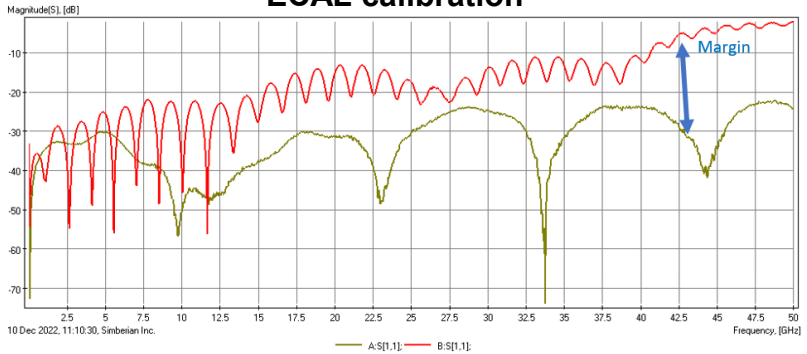




Sliding load calibration

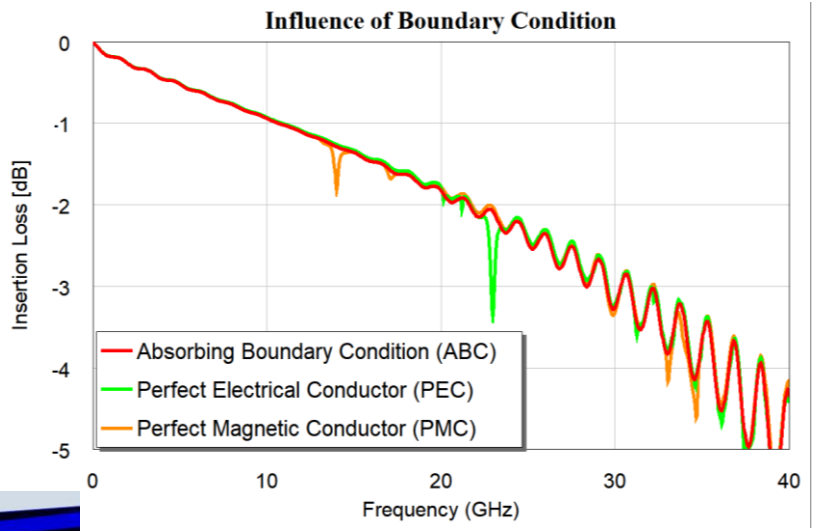


ECAL calibration



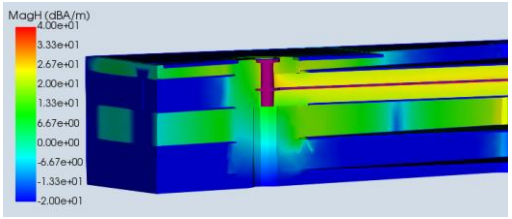
BOUNDARY INFLUENCE

- Boundaries must be carefully considered
  - Wrong placement → Influence on results
- Need to ensure
  - Boundary is sufficiently far away from the structure
  - Absorbing boundary conditions are useful for avoiding reflections

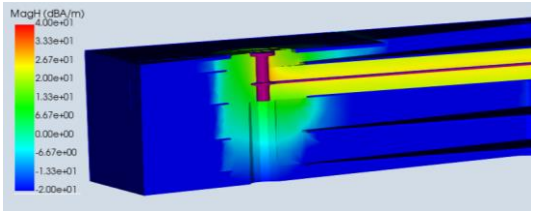


14 GHz Field Plots

Boundary Resonance (PMC)

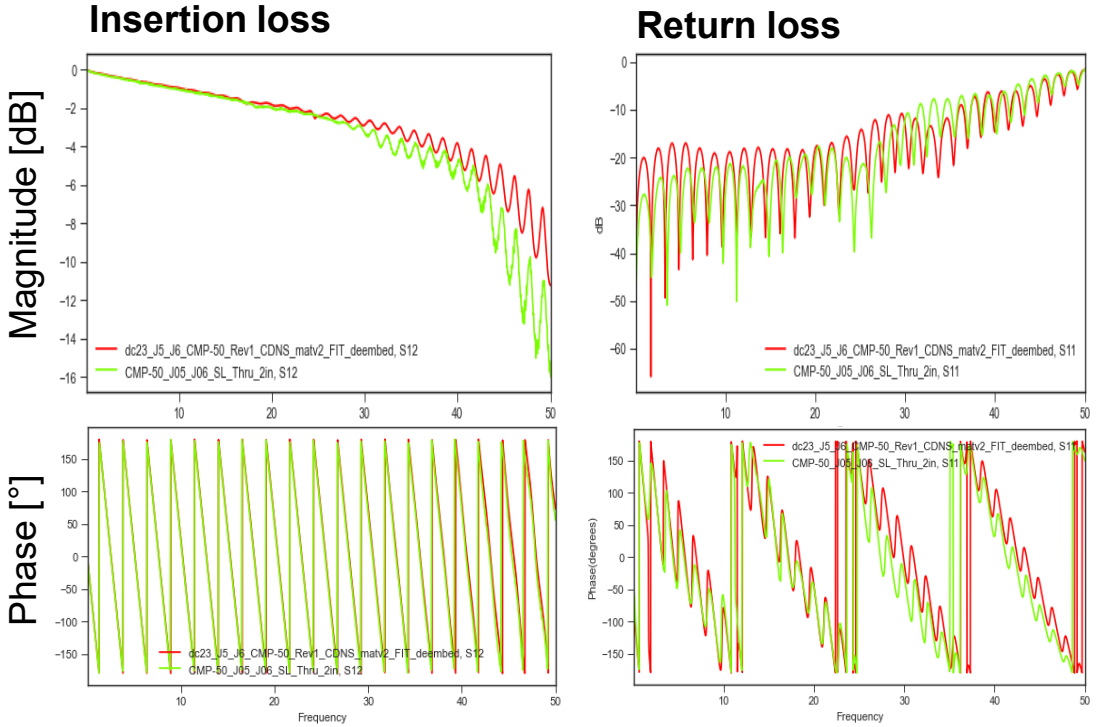


Absorbing boundary (ABC)



WHAT DO WE MEAN BY CORRELATION?

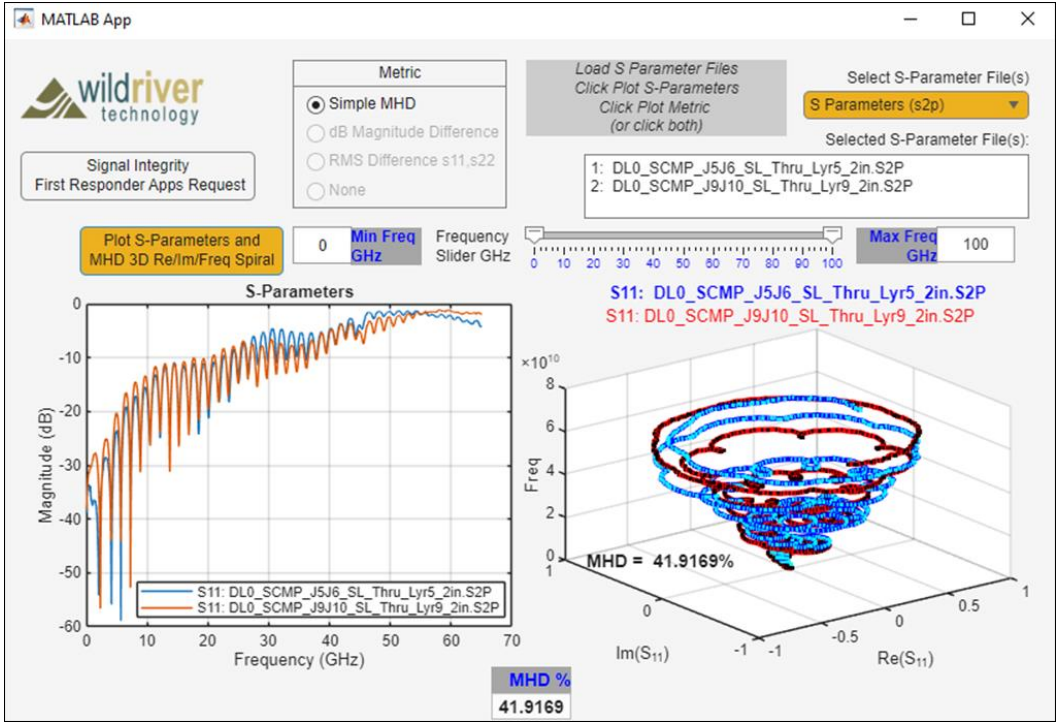
- 1:1 correspondence seldomly possible
- What is good correspondence?
- Which data set is “Golden” ? or are both “wrong” in different ways?
- Are my measurements perfect or Golden?
- What is Wrong with how we are doing Correspondence Analysis Today?



2” Stripline on DUT

A BETTER WAY – METRIC BASED COMPARISONS

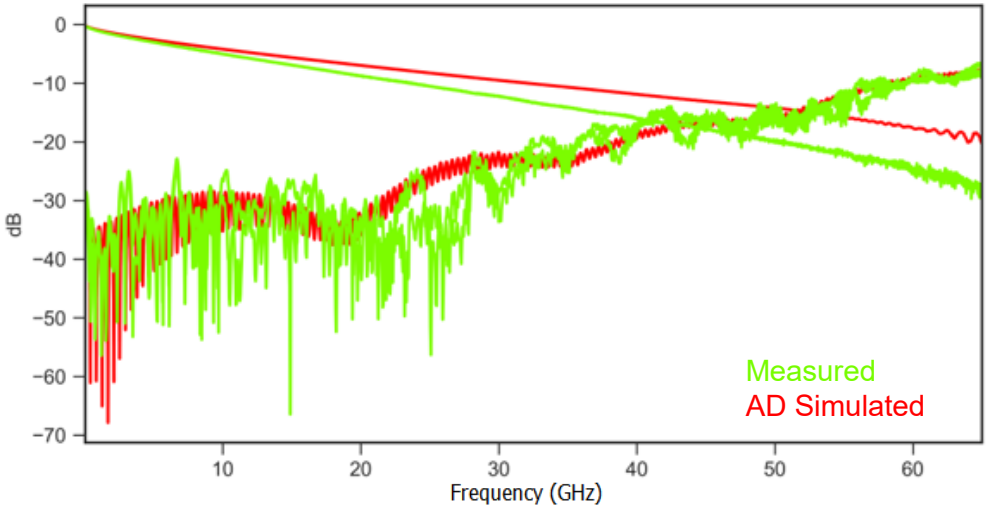
- Several metrics exists for s-parameter comparison, including IEEE FSV, Hausdorff, vector noms etc
- Example metric – Hausdorff:
  - quantifies minimum Euclidean distance in complex Real-Imaginary-Frequency (RIF) space
  - Metric is independent of sampling point differences
  - Equal weight on all S-parameter matrix entries
  - MHD similarity metric expressed correspondence between data sets from [0,100]



AS DESIGNED VS AS FABRICATED

- Example showing correlation from typical sign-off flow (red) vs measured measured board (green) from CMP70
- Simulation done based on best available information for sign-off in a typical design process
- Very good correlation on return loss
- Insertion loss suffers due to uncertainty mostly in surface roughness
- How much margin are you willing to allocate to such gap in your system budget?

8” Stripline, Full Path

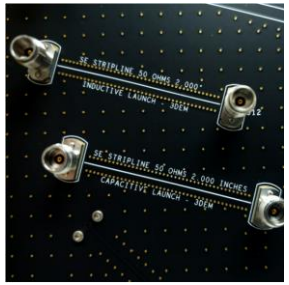


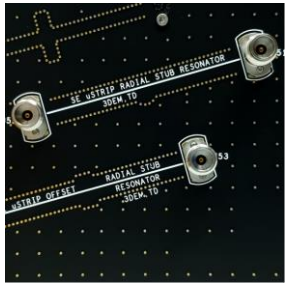
Hausdorff Figure of Merit			
	0-10GHz	0-35GHz	0-50GHz
S	62.4	61.8	63.3

Hausdorff = 0 (no correspondence)
Hausdorff = 100 (identical curves)

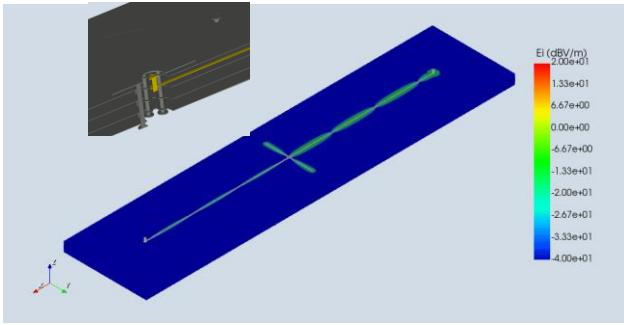
AS-FABRICATED SIMULATION = BETTER PREDICTABILITY

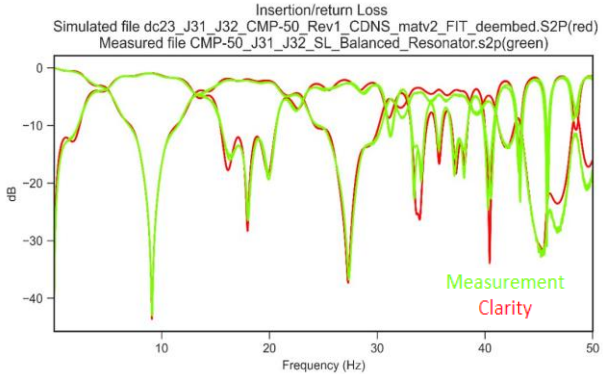
- Simulation based on material identification process and as-fabricated data
- Sample from Wild River Technologies CMP50 platform
- Full path extraction





Balanced Stripline Resonator

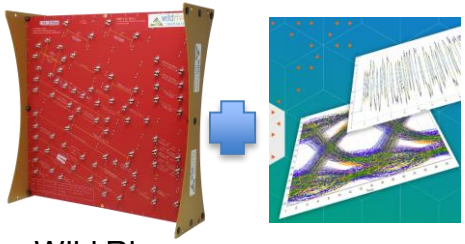




CadenceTECHTALK: Validating Clarity 3D Solver Accuracy Through Measurement Correlation

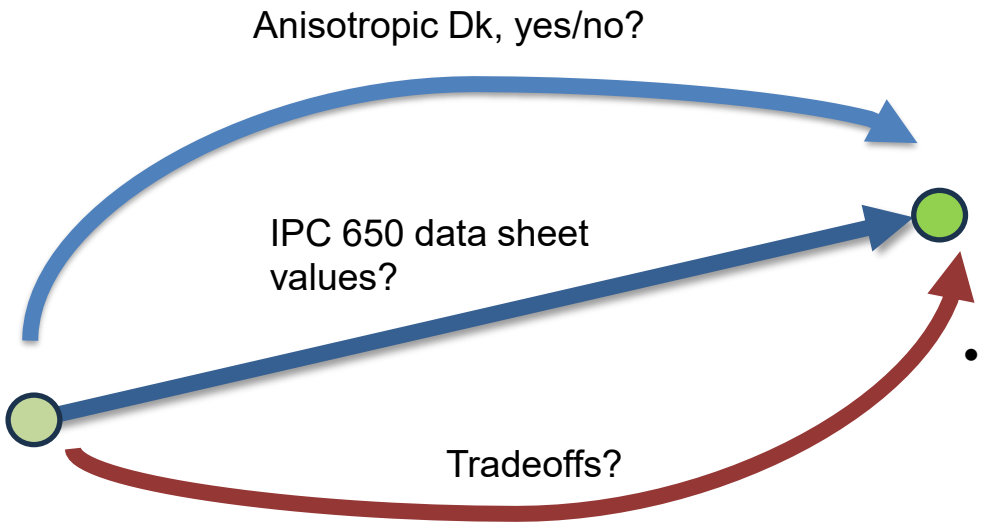
AN EXTREME SIGNAL-INTEGRITY VECTOR EXPERIMENT

How good is our simulation to measurement?



Wild River Tech CMP-70

Cadence Clarity

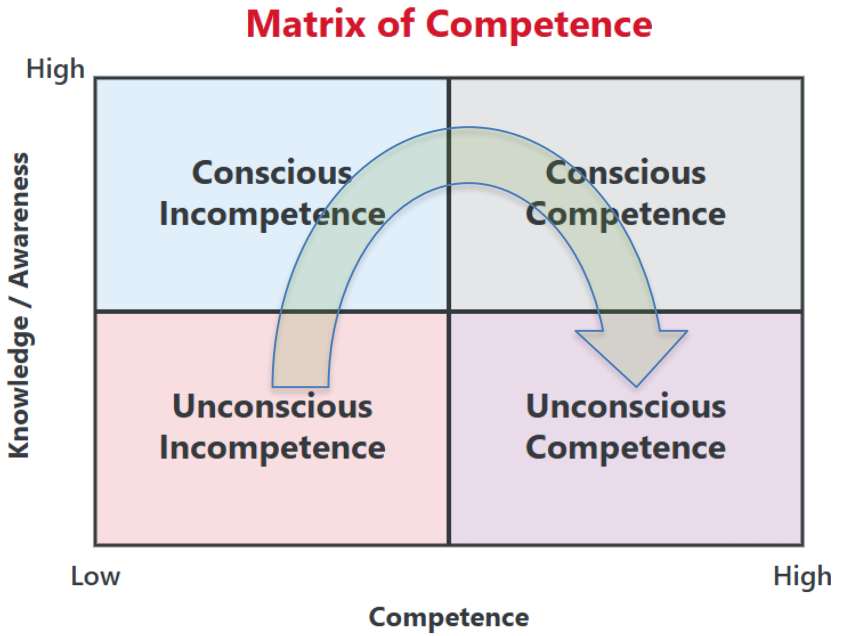


Improving material ID
Model possible paths

- ***Best practice to improve sim-to-measurement correlation with suitable material ID models***
- ***Based on system margin goal***

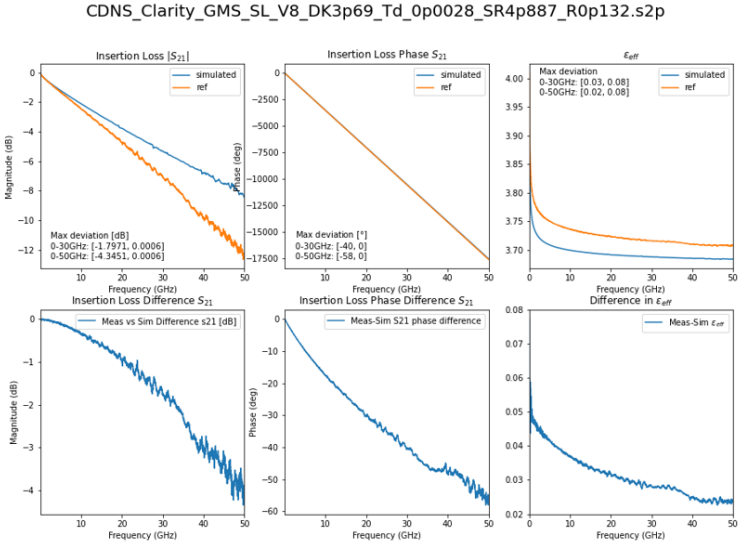
FUTURE PROOFING OUR FLOW

- What do we need to understand when going from 32G to 224G interfaces?
- What to consider / improve in our flow
  - Material identification
  - Anisotropic material behavior
  - Crosstalk
  - Statistical distribution of parameters
- Can we use datasheet values directly – what can we get away with – need to understand the problem and paths
- Technology is based on datarate and we will use rise and fall times as a metric
- Sensitivity vs design choices



MATERIAL IDENTIFICATION PROCEDURE

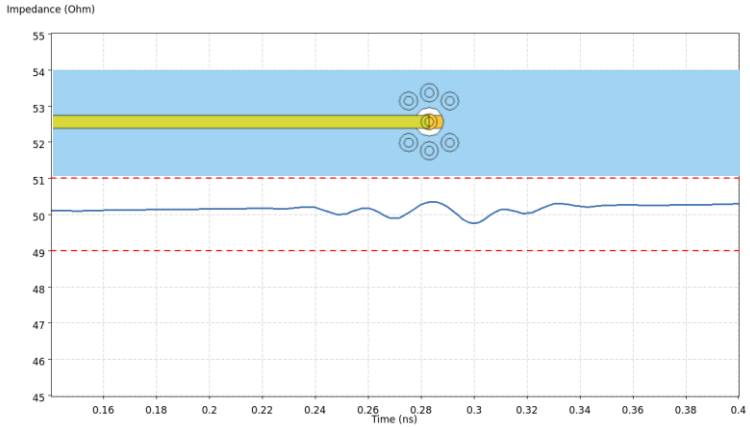
- Isotropic material identification based on 6” generalized s-parameter to de-embedded connectors (launches) from both simulation and measurements. Created from 2” and 8” lines on the test board
- Method of using AI/ML based tool for automated identification shown in *

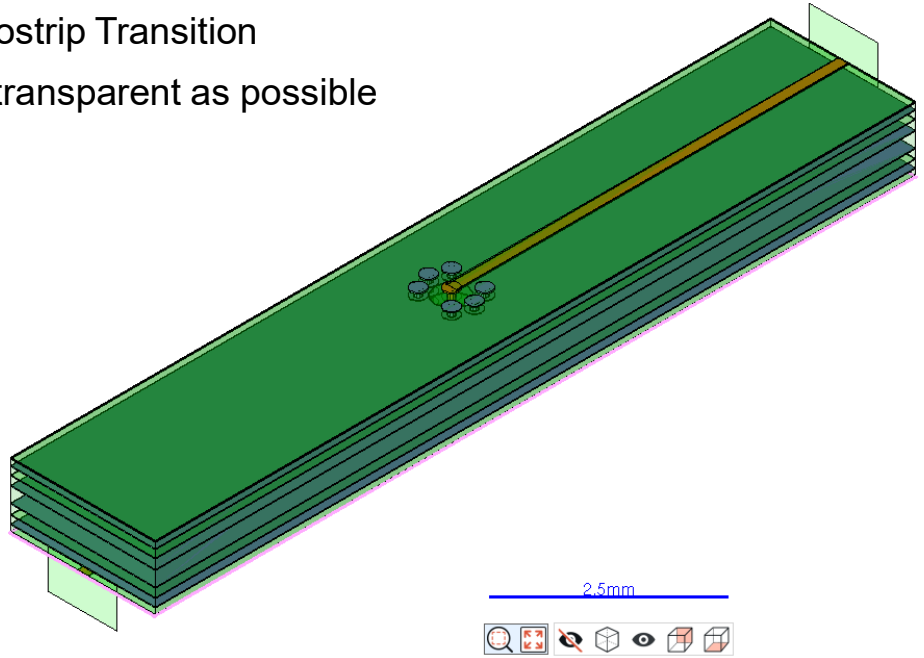


***Skytte et al “Free signal integrity? How understanding anisotropic materials and tolerances could increase performance at 112/224Gbps and beyond”, DesignCon 2025**

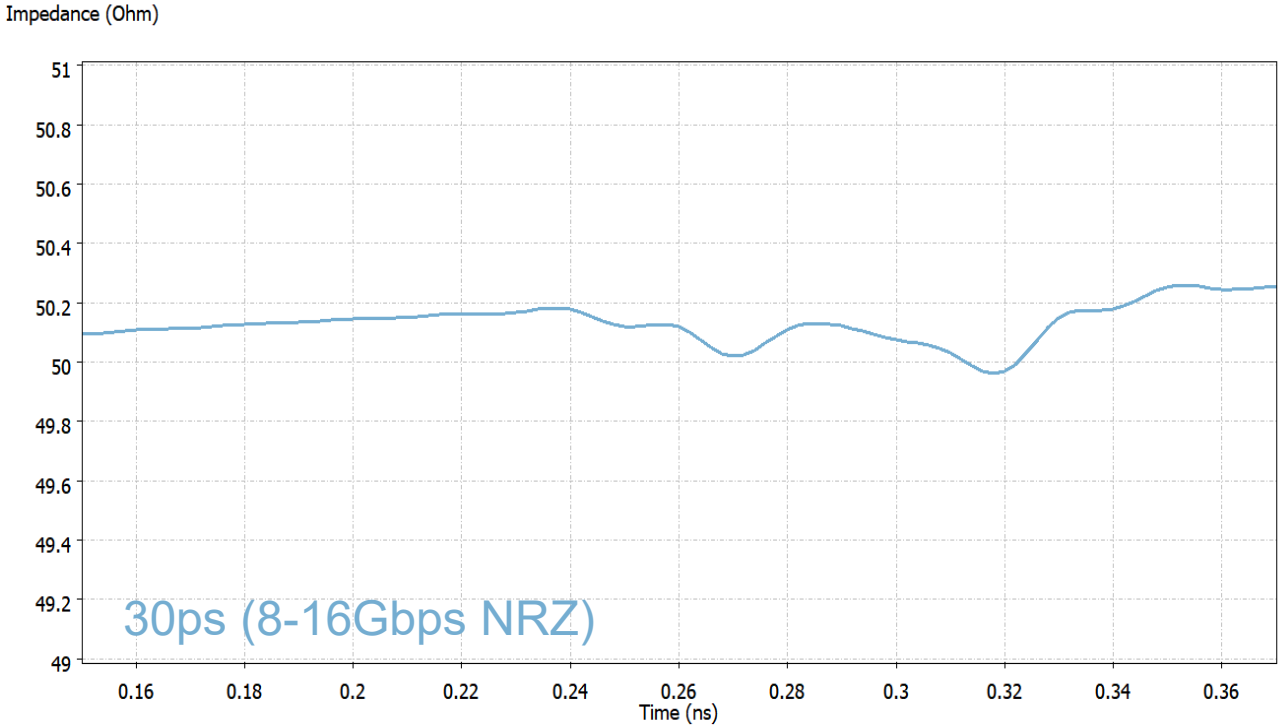
VECTOR STARTING POINT (REFERENCE DESIGN)

- DUT designed to explore variation vs material properties
- Geometry created from CMP50 – Microstrip to Microstrip Transition
- Started from As-Fabricated and optimized to be as transparent as possible

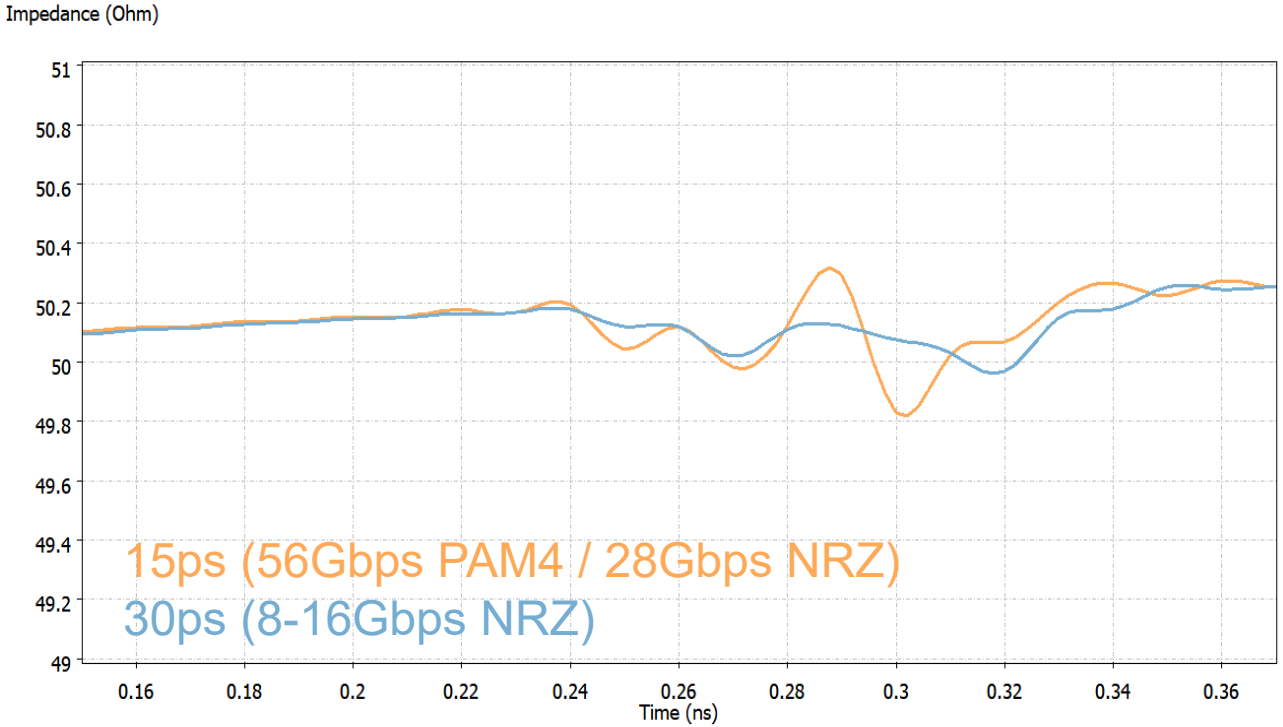




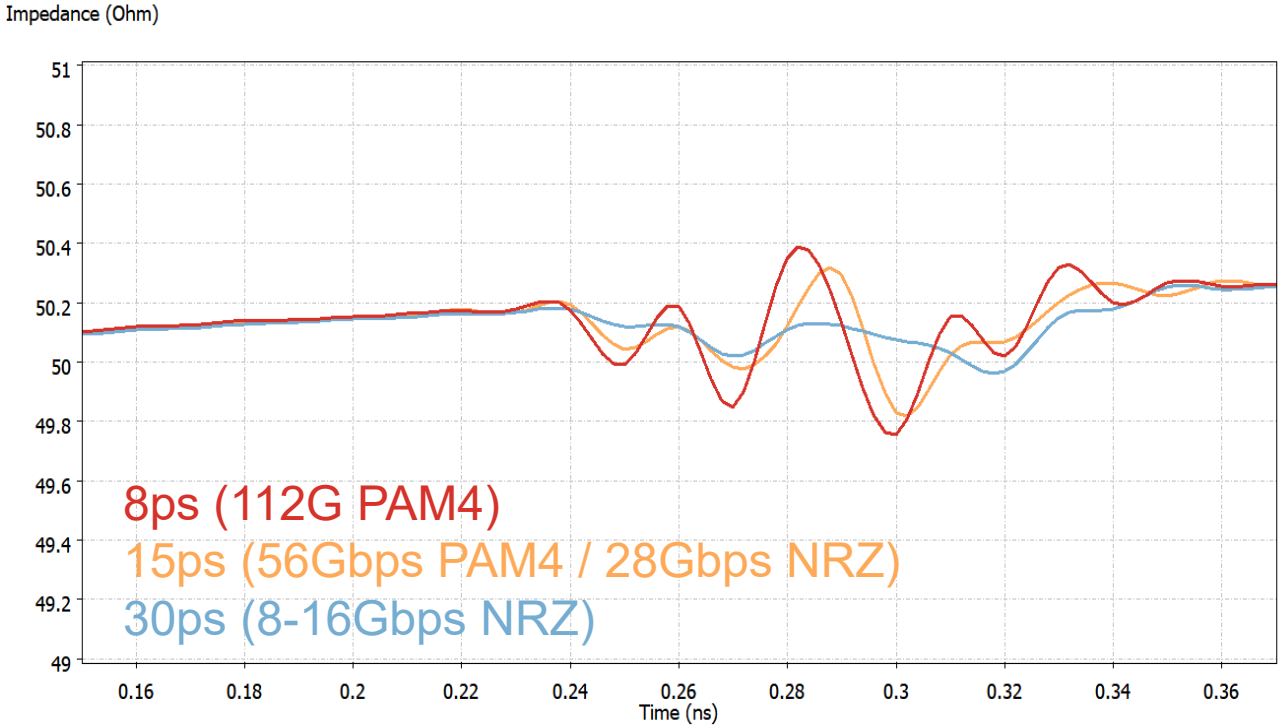
EXTREME SI LEADS TO …



EXTREME SI LEADS TO …



EXTREME SI LEADS TO LESS PAINFUL UPGRADE

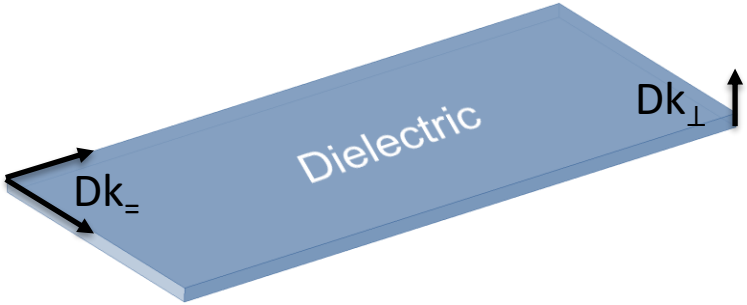


ANISOTROPY

- PCB is due to materials anisotropic
- We will assume uniaxial behavior: in-plane $Dk_{=}$, and out-of-plane $Dk_{\perp}$

$$\boldsymbol{Dk} = \begin{bmatrix} Dk_{=} & 0 & 0 \\ 0 & Dk_{=} & 0 \\ 0 & 0 & Dk_{\perp} \end{bmatrix}$$

- Most quoted numbers / datasheets assumes just ***ONE*** Dk value. Could be either of above or a mix for an effective / bulk Dk value
- Why could this be important?
  - $Dk_{=}$ for PCBs is typically higher than $Dk_{\perp}$ (Λ = 5-20)
  - Vias have significant out-of plane electrical fields
  - Fabriacted via might end up being more capacitive than expected

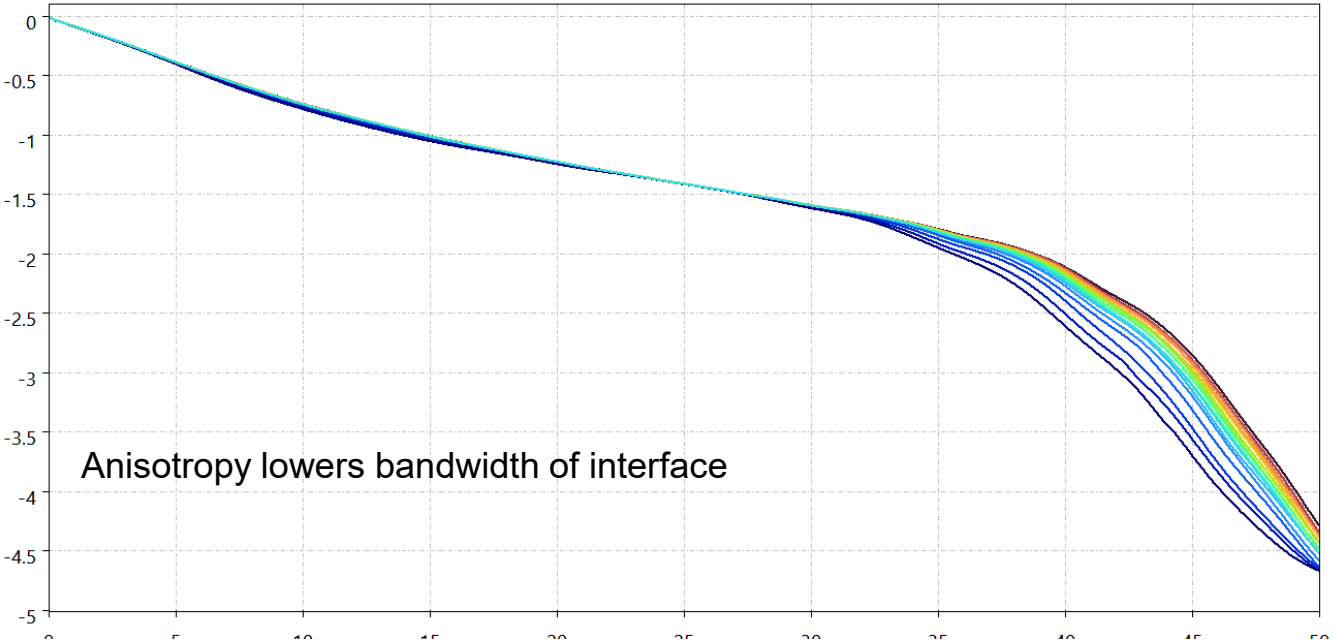


Level of anisotropy can be expressed as*

$$\Lambda = \left[\frac{Dk_{=}}{\mathrm{Dk}_{\perp}} - 1\right] * 100$$

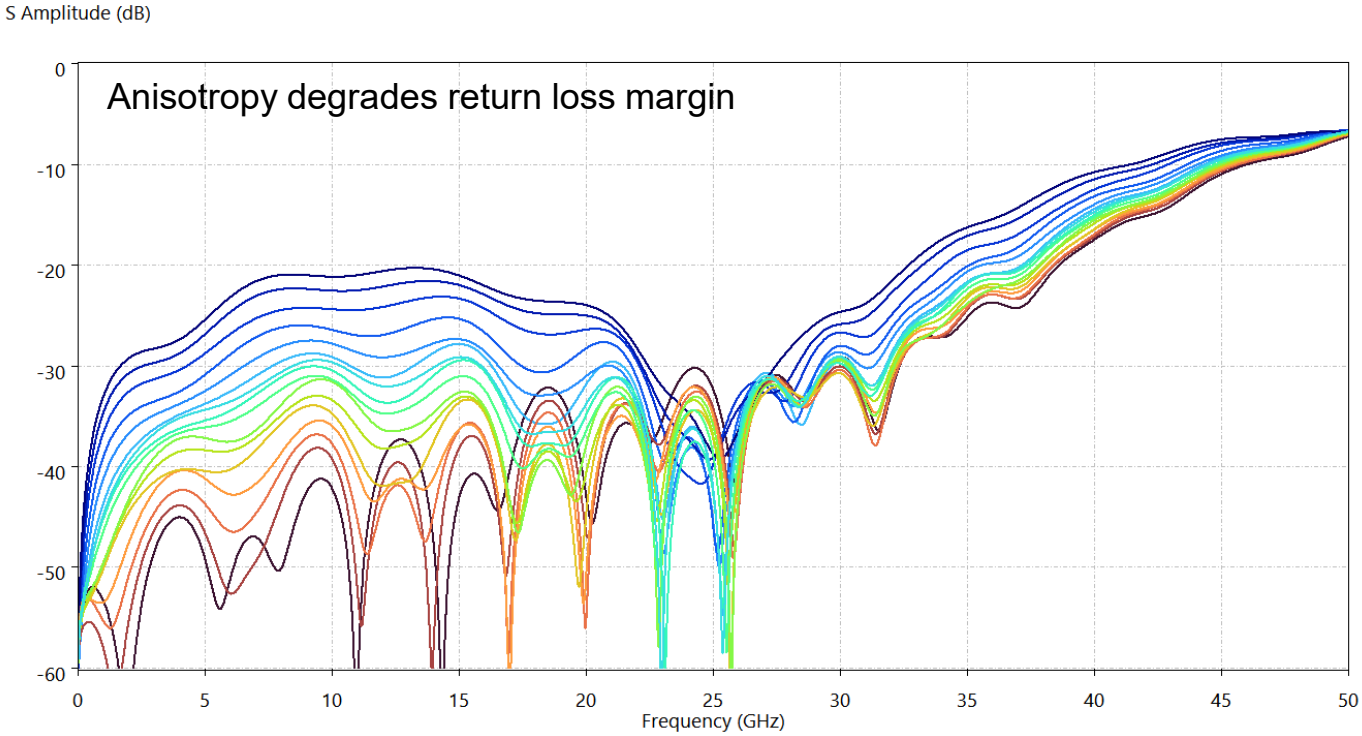
* L. Simonovich, "A Heuristc Approach to Assess Anistropic Properties of Glass Reinforced PCB Substrates," in *Designcon 2023*, Santa Clara, 2023.

VARIATION OF INSERTION LOSS WITH Λ



	LAMBDA
Case1	0
Case2	1
Case3	2
Case4	3
Case5	4
Case6	5
Case7	6
Case8	7
Case9	8
Case10	9
Case11	10
Case12	12
Case13	15
Case14	20
Case15	25
Case16	30

VARIATION OF RETURN LOSS WITH Λ



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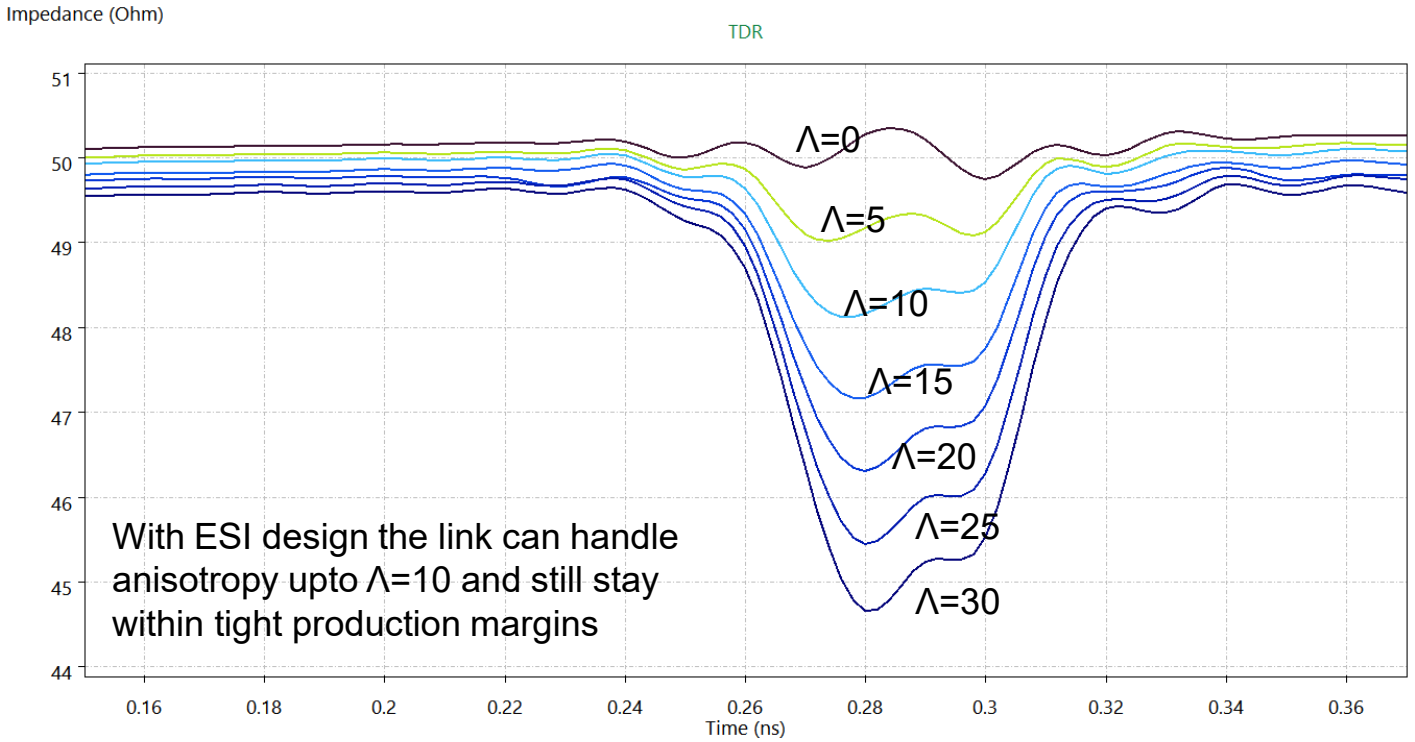
Case8	7
Case9	8
Case10	9
Case11	10
Case12	12
Case13	15
Case14	20
Case15	25
Case16	30

TDR VARIATION WITH Λ



	LAMBDA
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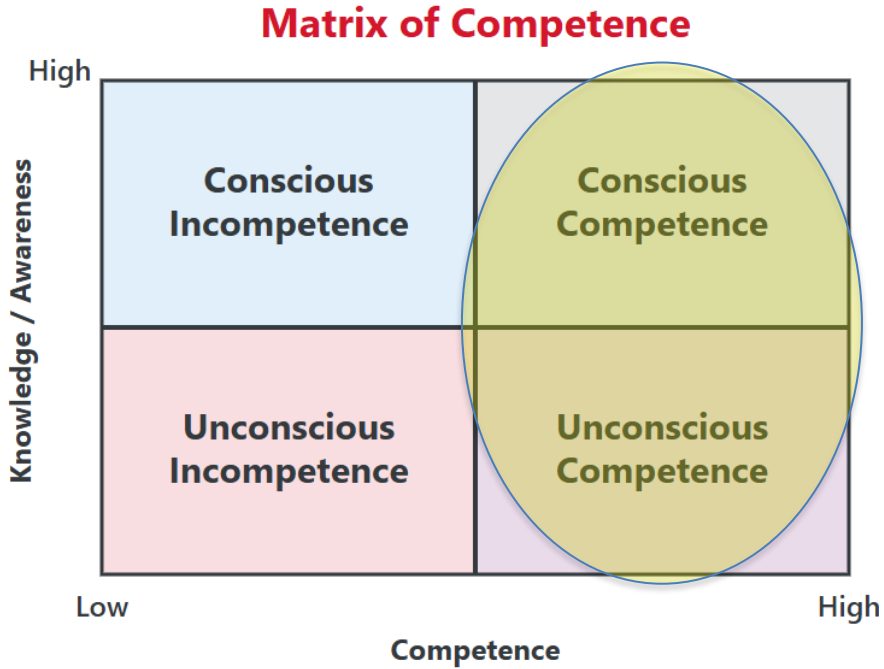
Case6	5
Case7	6
Case8	7
Case9	8
Case10	9
Case11	10
Case12	12
Case13	15
Case14	20
Case15	25
Case16	30

Summary

- Evolving an Extreme SI methodology
  - starts with a clear knowledge of where you are
  - where you need to be
  - the path(s) to success
- As Engineers we cannot rely solely on previous experience and unconscious competency we must always be re-evaluating our knowledge
- Establish strong vectors for success (defined by an end point based on your target technology)

Conclusion

- Our design methodology evolution should strive towards the right hand quadrants
- Exploring Vectors for Success is a key organizational tool



Thank you!

QUESTIONS?