RF Launch and Connector PCB Launch Design Signal Integrity Services

FEATURES

- RF launch design exceeds top tier IEEE 370 2020 for Extreme Signal Integrity
- Design Range: 40-110GHz
  - 2.92mm to 1.0mm
  - Edge and vertical mount
  - High Density like Bullseye
  - Custom connectors
- Achieve Extreme Signal Integrity for:
  - De-embedding
  - General Serial Link Test Fixtures
- Design Review with customer included
- WRT can assemble and do 100% NIST traceable TDR impedance testing

INCLUDES

- Mechanical Design of Connector to PCB
- Complete report
  - Optimization results in TDR and S-parameter
  - Geometries
  - DXF files
- Design Review web-meeting

OPTIONS

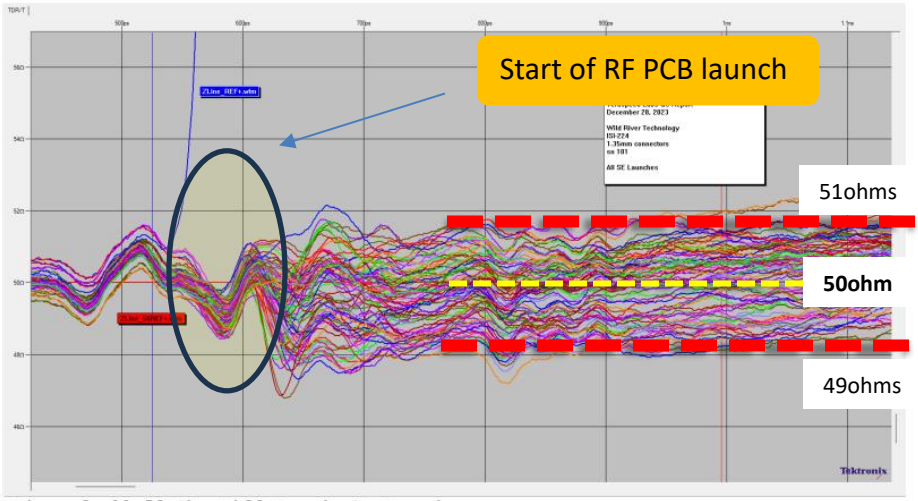
- Connector Model Testing and Report
- Generate 3D EM connector model
- Layout services
- Layout design review
- NIST traceable TDR testing of final assembled test fixture
- Design Stackup, insure DFM

Extreme Signal Integrity (ESI) Design Services

Wild River Technology's (WRT) Extreme Signal Integrity (ESI) design services are focused on customers whose applications demand the highest levels of signal integrity performance and who recognize the value of investing in a rigorous optimization process.

A key foundation of ESI performance is the optimization of RF launches and connector interfaces, which establish the signal integrity baseline for the entire test vehicle. WRT's engineering methodology leverages advanced 3D electromagnetic (EM) simulation and optimization techniques tailored to the specific objectives of each project—an industry-leading approach that differentiates WRT from conventional design practices.

RF optimization criteria vary depending on the intended application. For example, optimization targets for serial-link characterization differ significantly from those required for de-embedding structures. WRT designs to application-specific return-loss targets, ensuring that performance objectives are aligned with end-use requirements. Serial-link RF launch optimization is focused on the power spectral density associated with the intended data rate and encoding scheme, while de-embedding applications require broadband return-loss performance across a wide frequency range.



ZLine of all 50 Ohm Diff Boards SE Launches

RF launch TDR impedance measured is within 1ohm reflection, exceeding top-tier IEEE 370 2020 signal integrity. A TDR Impedance report of final assembled test fixture is available.

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PCB Launch Optimization Process

The WRT PCB launch optimization process begins with:

- Provide customer with budgetary quotation, get executive level acceptance to move forward from customer
- Signal Integrity Requirements Review – Conduct a detailed discussion to establish project-specific signal integrity objectives, which may include the complete test fixture architecture. The WRT engineering team provides guidance and recommendations for achieving Extreme Signal Integrity (ESI) performance based on Serial Link reach and margin, or other signal integrity metrics.
- Formal quotation and purchase order business
- Stackup Development and Evaluation – Review existing stackup definitions or develop new stackup that supports the desired material characteristics and optimization goals across the target frequency range.
- PCB Stackup Assessment – Analyze the PCB stackup for potential resonances, design-for-manufacturing (DFM) considerations, and overall suitability for achieving the specified ESI performance targets. This step is optional, based on performance requirements and existing stackup assessment from last step
- Obtain material properties for stackup laminate materials, including anisotropic Dk X-Y versus Z. This step is required for greater than 40GHz, 32G NRZ performance objectives (for example, it is required for 56G PAM4)
- Catalogue Design for Manufacturing Constraints (DFM)
- Perform 3D EM simulation, complete documentation package
- WRT internal review of simulated results
- WRT/customer formal design review
- WRT generates .dxf files
- WRT can assist or perform layout, optional
- WRT can assist with layout design review, WRT optionally can handle layout design as well
- WRT can assemble, do 100% NIST traceable TDR impedance analysis, generate report, customer team meeting to discuss

This disciplined process enables WRT to deliver highly optimized test vehicles and interconnect solutions tailored to the unique signal integrity requirements of advanced high-speed applications.

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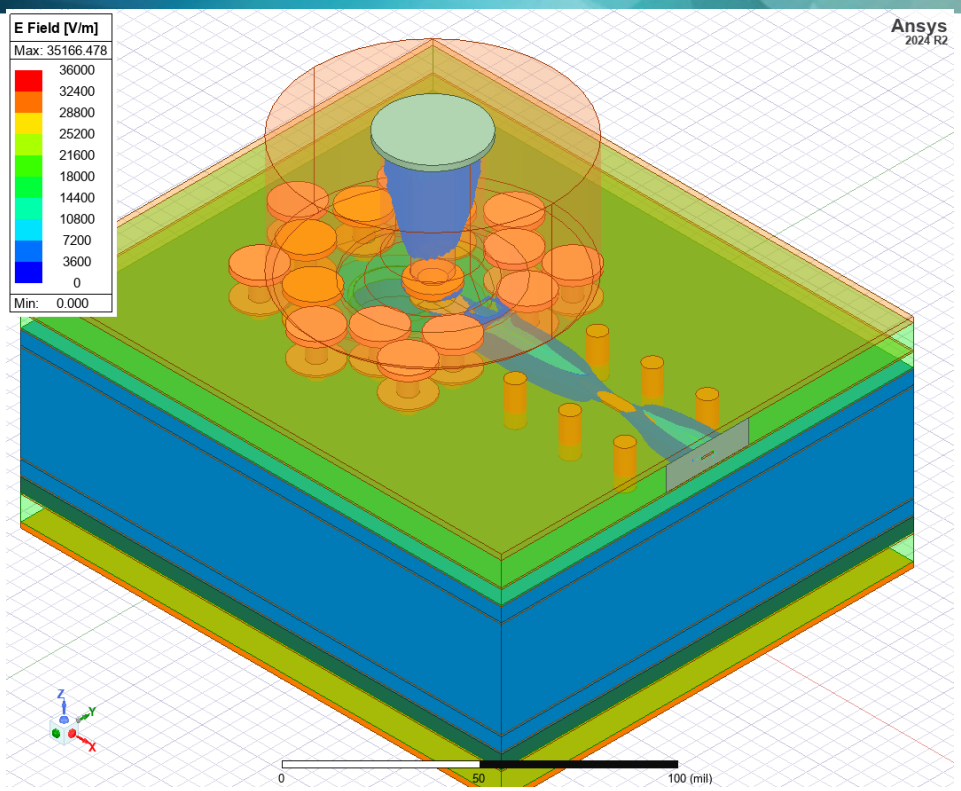
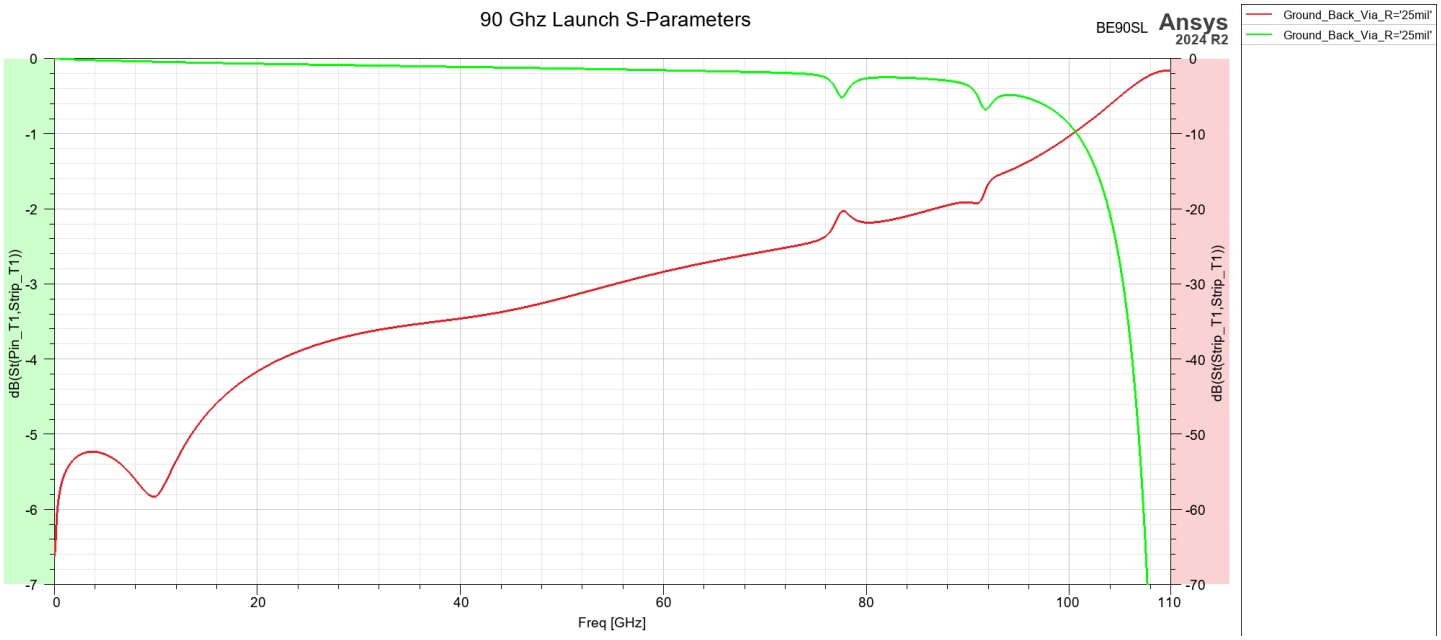
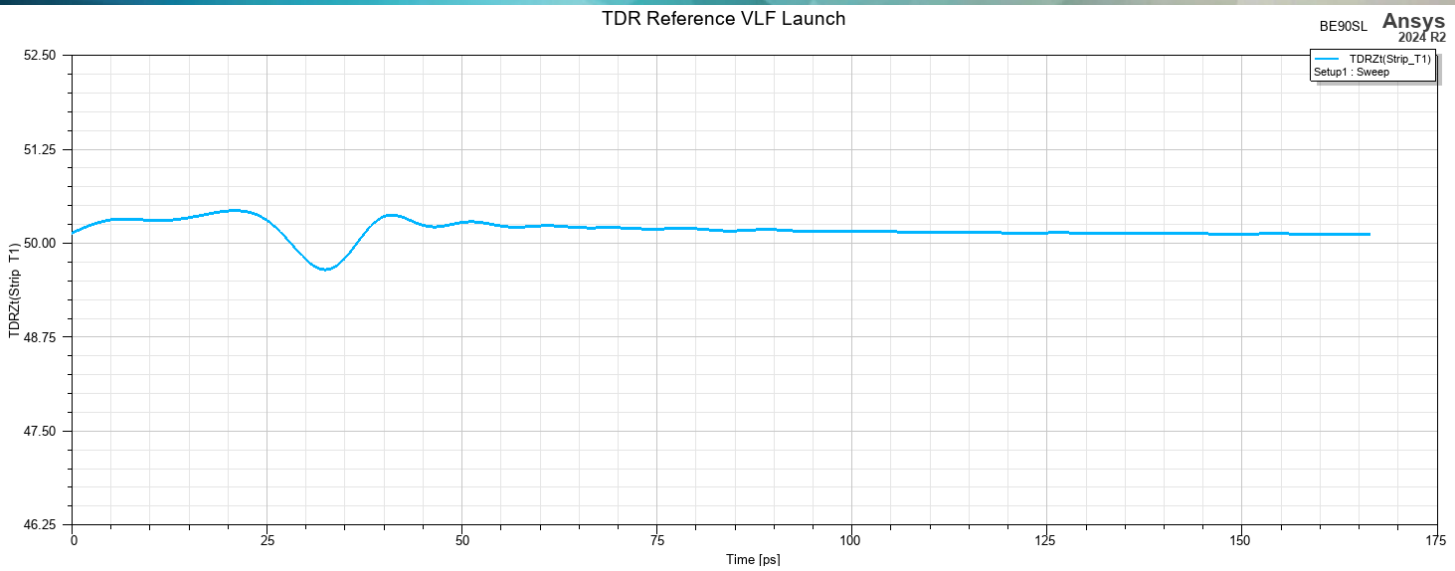


An integral part of the WRT RF PCB launch is isolation (localization is another used term). This determines two key Extreme SI factors:

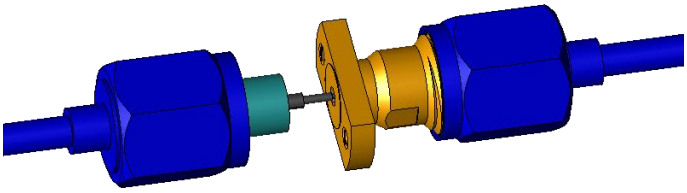
- Crosstalk aggression
- Control of impedance
- Mode and Resonance Management

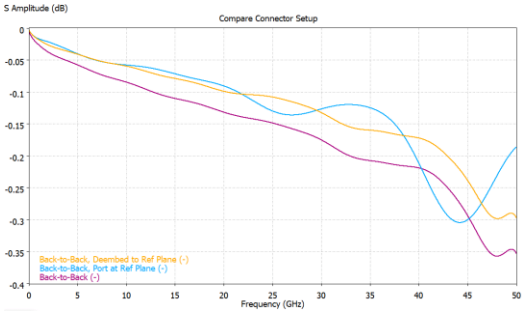


Example 110GHz RF launch optimization, first in frequency domain, and then time domain.

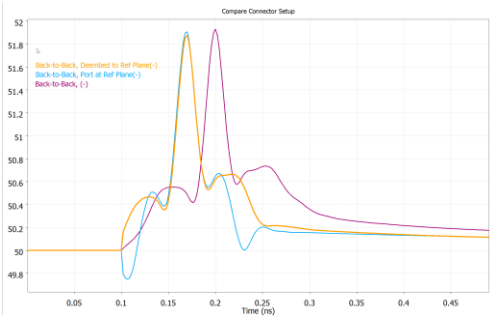


Below demonstrates an example of connector model testing conducted before the 3D EM optimization process. Note the TDR impedance bump shows excess inductance bump, which is desirable to compensate for via pad capacitance. Note that left hand connector metal body is hidden for illustration purposes.

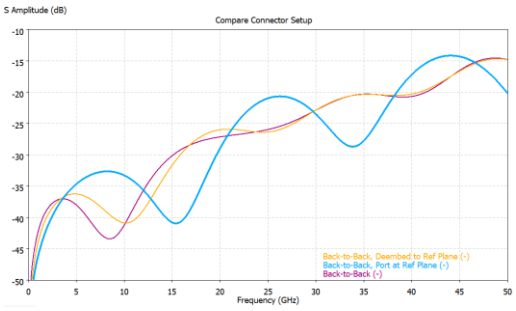




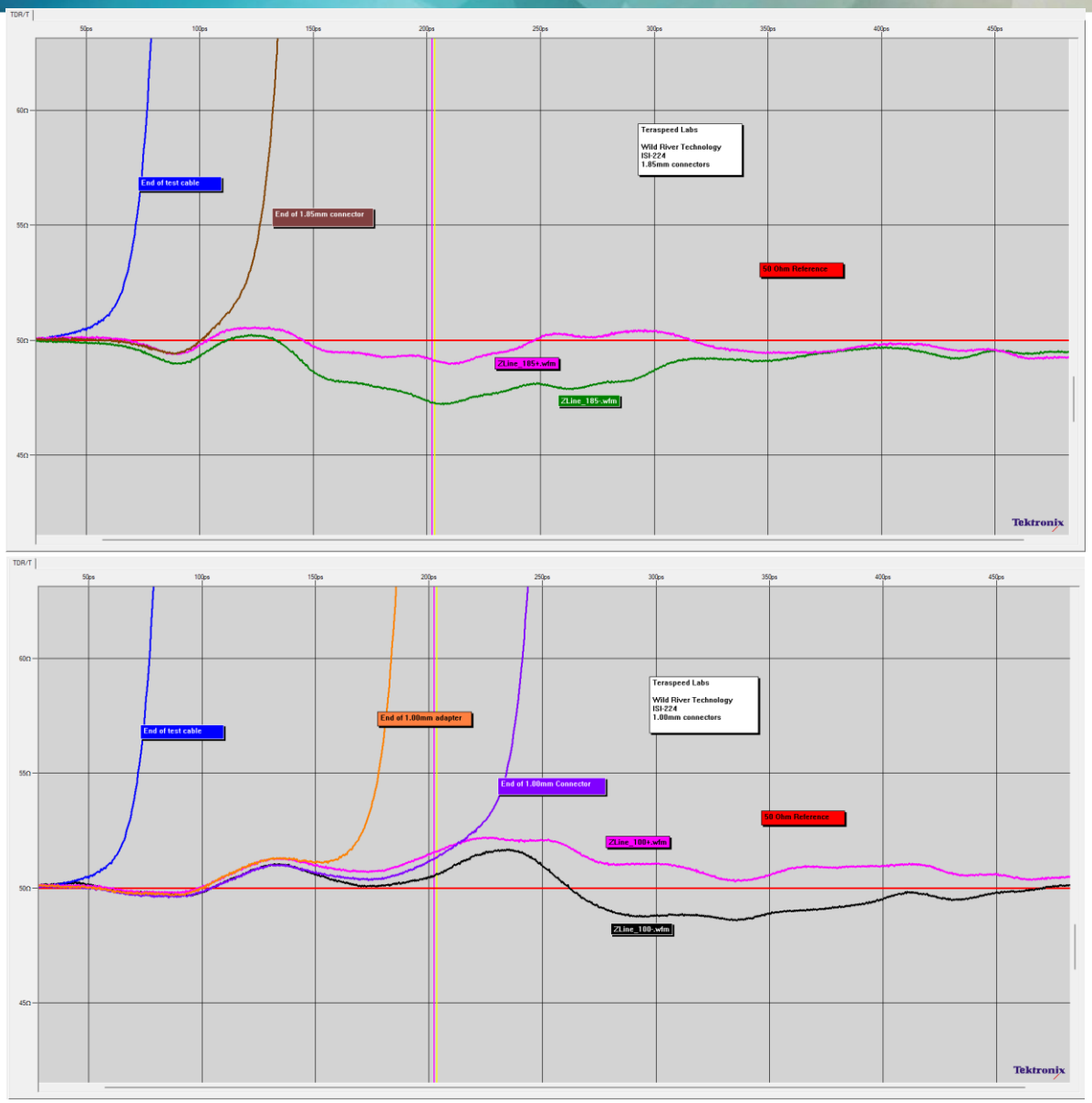
Insertion Loss [dB]



TDR Impedance

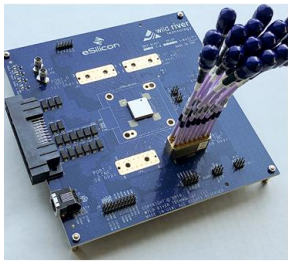


Return Loss [dB]

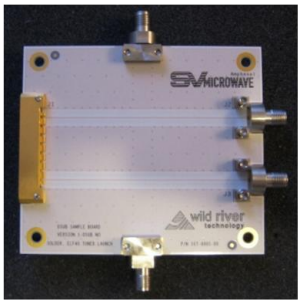


Examples of TDR impedance analysis, which is a optional post-assembled test service. These examples are from 1.85mm and 1.0mm measured TDR impedance from recent WRT projects.

Example RF launch optimization projects that yielded Extreme Signal Integrity

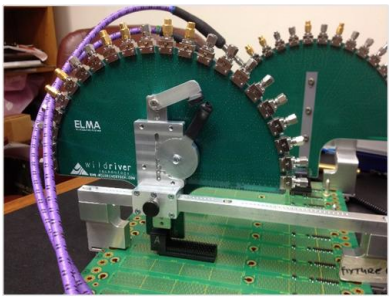


Samtec Bullseye 70



SW Microwave DSUB with edge launch

Vertical mount compression RF connector



RF edge launch for backplane testing

Optional Connector Model Validation Services

WRT also offers an optional connector model validation service to improve simulation accuracy and reduce development risk. Unfortunately, many commercially available connector models contain deficiencies that can adversely impact simulation results. Common issues include electrical inaccuracies, such as impedance discontinuities observed in TDR analysis, resonant behavior within the operating frequency range, and geometry-related problems that affect model integrity.

In addition, some models exhibit improper geometric healing or construction errors that can create meshing challenges for 3D electromagnetic (EM) field solvers, resulting in longer simulation times, reduced convergence, or inaccurate results.

As an additional validation option, WRT can incorporate dedicated measurement structures into the PCB design to enable correlation between simulation and measured performance. These structures provide a means to verify model accuracy, strengthen simulation-to-measurement correlation, and increase confidence in the overall signal integrity characterization process.

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Frequently Asked Questions:

Question: The connector companies often perform 3D EM optimization at no charge, why not just deal with them and not WRT?

Answer: The connector companies' ambition, as you would expect, is to service their connector sale. In contrast, the WRT team addresses a bigger scope with more intensity focused on Extreme Signal Integrity. Secondly, connector manufacturers usually skip model testing when optimizing pcb launches. The hasty approach can lead to frequent issues due model encryption, faulty material properties, and improper set up of the model. WRT maintains the integrity of the entire test fixture and offers optional 100% TDR impedance testing and assembly services. Also, WRT also provides proven mechanical mounting guidance so that macro-signal integrity is achieved. 100% NIST traceable TDR impedance testing of the assembled test fixture is also available.

Our objective at WRT is to provide Extreme Signal Integrity, not solve a technical problem enabling a connector sale.

Question: What are approximate costs?

Answer: $3400 for basic launch optimization to 50GHz, $4750 for 70GHz, $6800 for 90-110GHz. These prices are for top tier Extreme Signal Integrity and are only a starting point of costs. For Extreme Signal Integrity we often must either review the customer stackup or create one. A non-optimal stackup hobbles the RF launch design into the PCB.

Question: What is included in the package?

Answer: Comprehensive report outlining pcb launch geometries, S-parameters, TDR impedance, summary of stackup and any DFM issues, meeting with customer to review, dxf files.

Question: Have you had issues with getting models from connector vendors?

Answer: Not usually. WRT can optionally create a 3D EM model of the connector, which usually is a better model than the vendor supplied encrypted version.

Question: We need help with other elements of the test fixture, can you help with that?

Answer: Yes, we start with a simple Statement of Work that we help customers to create. Often customers don't see the issues that are critical to Signal Integrity, we help with that. An example is crosstalk, another is possibility to mode or resonance.

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Question: We don't have a stackup, can you help us create one?

Anwer: Yes, we can. The WRT team also addresses manufacturability, Design for Manufacturing or DFM, both power and high-speed design potential of the stackup. Often, we can provide a proven stackup from our test fixture library of stackup designs.

Contact Alexa Bell at Alexa@wildrivertech.com to schedule a brief meeting to start the Statement of Work process. Typically, an NDA is required which Alexa also manages.